NANO-8050

NANO-ITX Board

User's Manual

Version 1.0

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Appendix A

Appendix B

How to Use This Manual

The manual describes how to configure your system board to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Host Board.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single host board.

Chapter 2 : Hardware Configuration. Shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3 : System Installation. Describes how to properly mount the CPU, main memory and Compact Flash to get a safe installation and provides a programming guide of Watch Dog Timer function.

Chapter 4 : BIOS Setup Information. Specifies the meaning of each setup parameters, how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give users some guidelines of trouble-shooting.

Chapter 5 : Troubleshooting. Provides various useful tips to quickly get its running with success. As basic hardware installation has been addressed in Chapter 3, this chapter will basically focus on system integration issues, in terms of backplane setup, BIOS setting, and OS diagnostics.

The content of this manual is subject to change without prior notice. These changes will be incorporated in new editions of the document. **Portwell** may make supplement or change in the products described in this document at any time.

Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site : http://www.portwell.com.tw/.

Chapter 1
System Overview

1.1 Introduction

Portwell Inc., a world-leading innovator in the Industrial PC (IPC) market and a member of the Intel® Communications Alliance, has launched its new NANO-ITX form factor based NANO-8050 in response to market demand for a high performance embedded system board (ESB) that combines a smaller footprint, lower power consumption, and with longevity support.

Adopt with Intel® Core 2 Duo and Celeron ULV BGA type processors, NANO-8050 can provide higher performance but in small form factor.

NANO-8050 series supports dual displays, such as VGA port up to 2048 x 1536 resolution and dual channel 24 bit LVDS port. It supports one 200-pin SODIMM memory slot for DDR2 up to 2GB, and comes with single Gigabit Ethernet ports, one COM port, two SATA 300 ports (RAID 0,1), one Compact Flash socket, and Six USB2.0 ports. It also equipped with audio codec that supports one Mic in and Line out Jack.

Advanced Management Technology (AMT) 4.0 is feature that NANO-8050 with Core 2 Duo processors equipped (Celeron processors not support). This technology provides remote access capability via Intel® Gigabit Ethernet controller. The new technology is a hardware-based solution that uses out-of-band communication for system management access to client systems. Built in Intel® Trusted Platform Module (iTPM) technology that can enhance platform security.

NANO-8050 series brief specifications:

- Support Intel® Core 2 Duo, Celeron ULV processors in BGA type with FSB 1066/800MHz
- One 200-pin DDR2 SODIMM socket, support for DDR2 800/667 up to 2GB system memory
- Intel® GS45 integrated GMA 4500MHD that support DirectX 10, OpenGL 2.0, MPEG-2 hardware acceleration
- Equipped single Gigabit Ethernet port
- Support one Compact Flash socket, one COM port, two SATA ports and Six USB 2.0 ports (four ports on rear I/O)

1.2 Check List

The NANO-8050 series package should cover the following basic items

- ✓ One NANO-8050 NANO-ITX Main board
- ✓ One Active or Passive CPU cooler/heatsink
- ✓ One ATX power cable
- ✓ One Installation Resources CD-Title

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

1.3 Product Specification

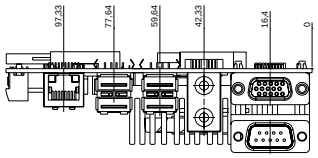
- **Main processor**
  - Support Intel® Core 2 Duo processors: SP9300 (2.26GHz), SL9400 (1.86GHz), SU9300 (1.2GHz) & Celeron ULV processors: ULV 722 (1.2GHz), ULV723 (1.2GHz)
  - CPU bus clock: 1066/800 MHz
- **Chipset**
  Intel® GS45 and ICH9M SFF (Small Form Factor)
- **Main Memory**
  - Support single channel DDR2 memory interface
  - Up to 2GB DDR2 SODIMM on one 200-pin memory socket
- **System BIOS**
  AMI BIOS
- **Expansion Interface**
  One PCI-Express x 1slot
- **SATA Interface**
  Two SATA ports support RAID 0, 1
- **Serial Ports**
  Support one RS232/422/485 selectable serial port
- **USB Interface**
  Support six USB (Universal Serial Bus) ports (four USB ports on rear I/O)
- **Compact Flash**
  - Support one Type II Compact Flash socket (up to UDMA5 mode)
  - Support boot from Compact Flash function
- **Audio Interface**
  - On board Audio codec via HD Audio interface
  - One Audio Jack on rear I/O for Mic in/Line out

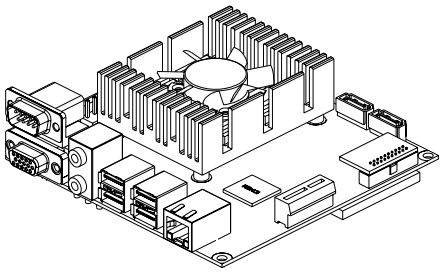
- **Auxiliary I/O Interfaces**
  System reset switch, external speaker, and HDD active LED, etc
- **Real Time Clock/Calendar (RTC)**
  Support Y2K Real Time Clock/Calendar with battery backup for 7-year data retention
- **Watchdog Timer**
  - Support WDT function through software programming for enable/disable and interval setting
  - Generate system reset
- **On-board VGA**
  - Intel® GMCH Integrated 4500MHD Graphics device
  - Intel® DVMT 5.0 supports up to 128MB video memory
- **On-board Ethernet LAN**
  Intel® 82567LM Gigabit Ethernet controller to support one RJ-45 connector on rear I/O
- **High Driving GPIO**
  Onboard programmable 8-bit Digital I/O interface
- **Cooling Fans**
  Support one 3-pin header for CPU fan
- **Outline Dimension (L X W):**
  120mm (4.72") X 120mm (4.72")
- **Power Requirements:**
  Power Consumption test: Run Burning Test V5.3, RUN time: 10 / 30 Minutes.
  +12V (System) @ 1.0A
  +5V (System) @ 4.5A
- **Configuration:**

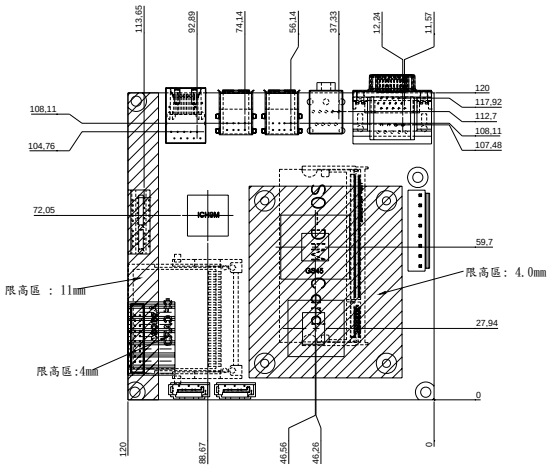
System Configuration	
CPU Type	Intel® Core™ 2 Duo CPU U9300 @1.20GHz L2:3072K FSB:800MHz
SBC BIOS	Portwell,Inc. NANO-8050 Rev.:R1.00.E0 (09022009)
Memory	Transcend DDR2 667 2GB (美光 7TE17D9HNL)
VGA Card	Onboard Intel® GS45 Express Chipset
VGA Driver	Mobile Intel® 4 Series Express Chipset Version 6.14.10.5039
LAN Card	Onboard Intel® 82567LM Gigabit Network Connection
LAN Driver	Intel® 82567LM Gigabit Network Connection Version 9.52.9.0
Audio Card	Onboard Realtek ALC262 Audio Chipset
Audio Driver	Realtek High Definition Audio Version 5.10.0.5794
Chip Driver	Intel® Chipset Device Software Version 9.0.0.1008
USB 2.0 Driver	Intel® ICH9 Family USB2 Enhanced Controller Version 8.3.0.1011
SATA HDD	Seagate ST3120813AS 120GB
Compact Flash	Apacer 128MB
CDROM	LITE-ON LH20A1S DVD-ROM
Power Supply	Portwell, Inc PW-330ATXE-12V

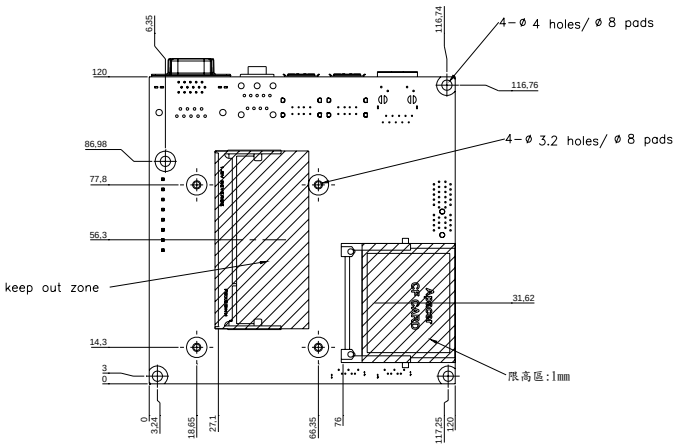
- **Operating Temperature:**
  0°C ~ 60°C
- **Storage Temperature:**
  -20°C ~ 80°C
- **Relative Humidity:**
  5% ~ 90%, non-condensing

1.3.1 Mechanical Drawing



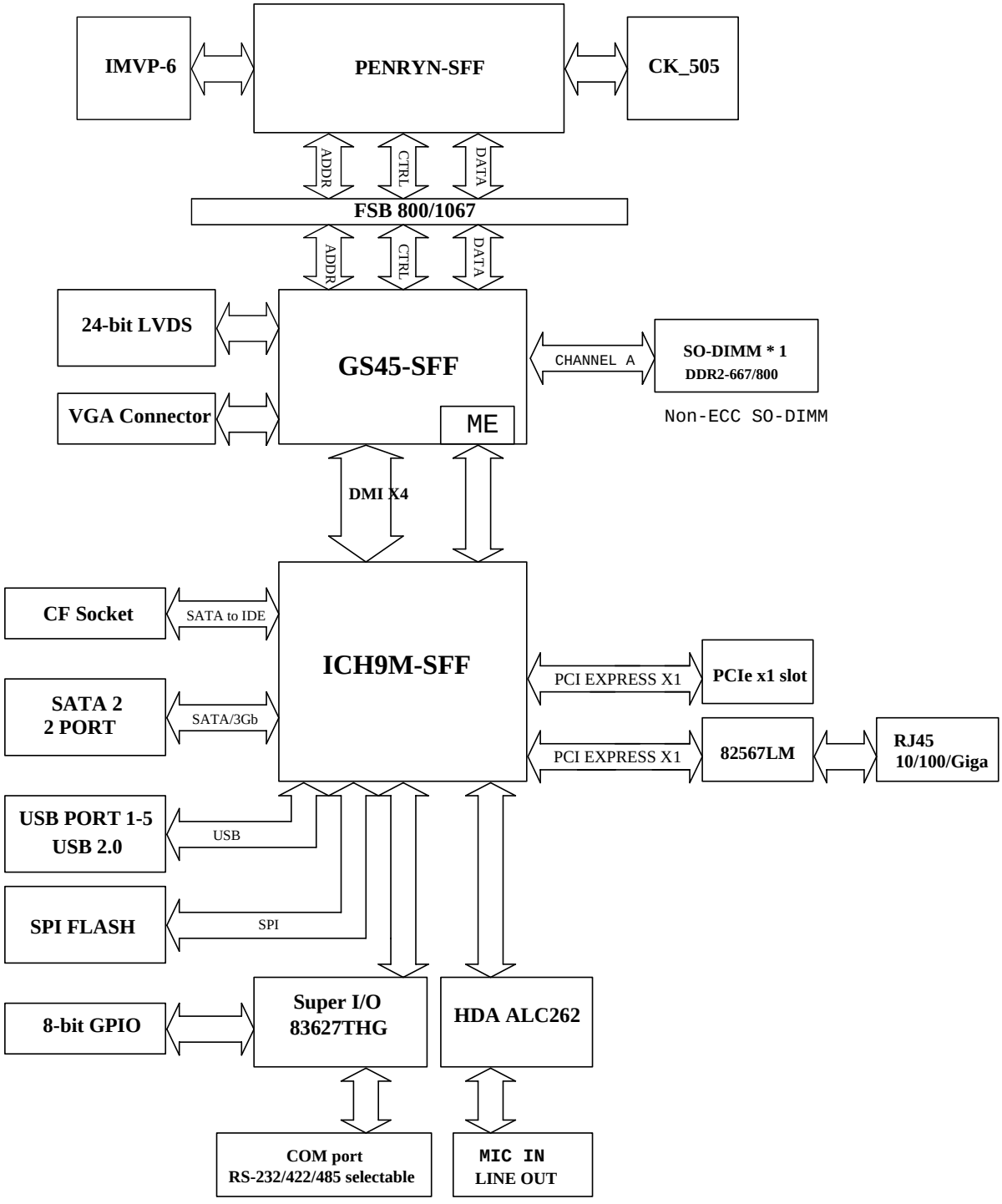






1.4 System Architecture

All of details operating relations are shown in NANO-8050 System Block Diagram.



NANO-8050 System Block Diagram

Chapter 2
Hardware Configuration

This chapter gives the definitions and shows the positions of jumpers, headers and connector. All of the configuration jumpers on NANO-8050 are in the proper position. The default settings are indicated with a star sign (★).

2.1 Jumper Setting

In the following sections, **Short** means covering a jumper cap over jumper pins; **Open** or **N/C** (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 2-1 for the Jumper allocations.

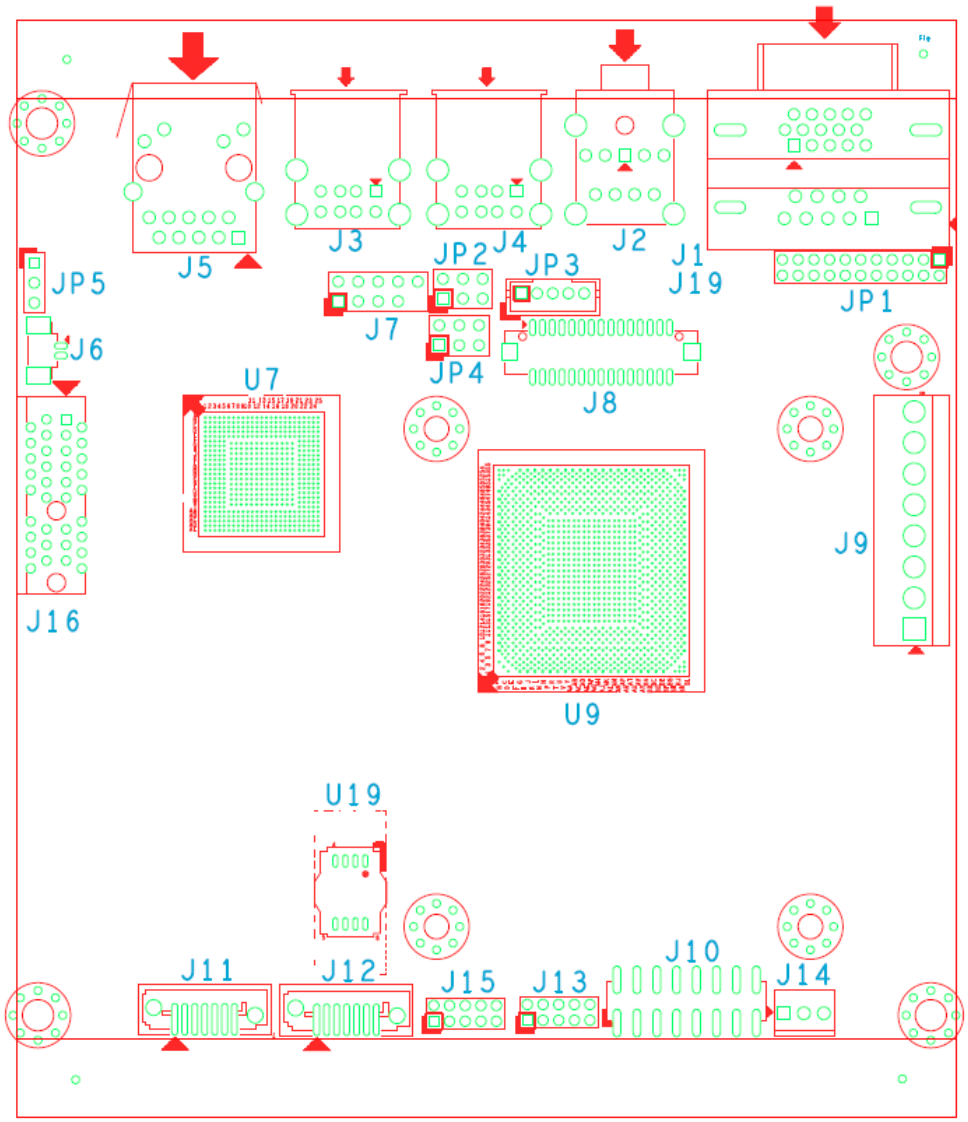


Figure 2-1 NANO-8050 Jumper and Connector Locations

JP1 : COM1 Port Interface Selection

JP1	Function
5-6,9-11,10-12,15-17,16-18 Short	RS-232 ★
3-4,7-9,8-10,13-15,14-16,21-22 Short	RS-422
1-2,7-9,8-10,19-20 Short	RS-485

JP2 : LVDS Power

JP2	Function
1-2 Short	3.3V ★
3-4 Short	12V
5-6 Short	5V

JP3 : LVDS Inverter Connector

PIN No	Signal Description
1	Back light enable
2	GND
3	VCC12
4	GND
5	VCC

JP4 : JP4LVDS Back light Power

JP4	Function
1-3 Short ; 2-4 Short	Active High 5V ★
1-3 Short ; 4-6 Short	Active High 12V
3-5 Short ; 2-4 Short	Active Low 5V
3-5 Short ; 4-6 Short	Active Low 12V

PS. Current spec. supports up to 0.5A

JP5 : RTC Reset

JP5	Function
1-2 Short	Normal Operation ★
2-3 Short	Clear CMOS

2.2 Connector Allocation

I/O peripheral devices are connected to the interface connectors

Connector Function List

Connector	Description	Remark
J1	On-board VGA CRT Connector	
J2	Audio Connector	
J3	USB 0/1 Connector	
J4	USB 2/3 Connector	
J5	RJ-45	
J6	Battery Connector	
J7	USB 5/6 Pin Header	
J8	LVDS Connector	
J9	ATX Power Connector	
J10	1-7:Buzzer, 9-11: Power Bottom, 13-15:Reset, 2-4: SUS_LED, 6-8:PLED 14-16: SATA LED	
J11	SATA Connector	
J12	SATA Connector	
J13	GPIO Connector	
J14	Fan Connector	
J15	PS2 K/M Pin Header	
J16	PCI-E*1 Connector	
J17	DDR2 SO-DIMM	
J18	CF Connector	
J19	On-board COM. Connector	

Pin Assignments of Connectors

J1 : On-board VGA CRT Connector

PIN No.	Signal Description
1	Red
2	Green
3	Blue
4	Monitor ID0 (MONID0) (5V I/F)
5	Ground
6	Ground
7	Ground
8	Ground
9	+5V

10	Ground
11	Monitor ID1 (MONID1) (5V I/F)
12	VGA DDC Data (5V I/F)
13	Horizontal Sync. (HSYNC) (5V I/F)
14	Vertical Sync. (VSYNC) (5V I/F)
15	VGA DDC Clock (5V I/F)

J2 : Audio Connector

PIN No.	Signal Description	PIN No.	Signal Description
Green	LINE_OUT	Pink	MIC_IN

J3/J4 : USB Connector

PIN No.	Signal Description	PIN No.	Signal Description
J3	USB port0	J4	USB port2
J3	USB port1	J4	USB port3

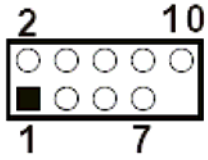
J5 : RJ45 Connector

PIN No.	Signal Description
RJ45	100/Giga network

J6 : Battery Connector

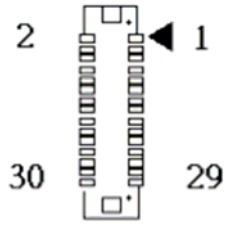
PIN No.	Signal Description	PIN No.	Signal Description
1	Battery +	2	Battery -

J7 : USB Header



PIN No.	Signal Description	PIN No.	Signal Description
1	5V Dual	2	5V Dual
3	USB-	4	USB-
5	USB+	6	USB+
7	Ground	8	Ground
9	NC	10	Ground

J8 : LVDS Interface Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	LVDSA_DATA0	2	LVDSA_DATA0#
3	LVDSA_DATA1	4	LVDSA_DATA1#
5	LVDSA_DATA2	6	LVDSA_DATA2#
7	LVDSA_DATA3	8	LVDSA_DATA3#
9	LVDSA_CLKP	10	LVDSA_CLKN
11	LVDSB_DATA0	12	LVDSB_DATA0#
13	LVDSB_DATA1	14	LVDSB_DATA1#
15	LVDSB_DATA2	16	LVDSB_DATA2#
17	LVDSB_DATA3	18	LVDSB_DATA3#
19	LVDSB_CLKP	20	LVDSB_CLKN
21	DDC_DATA	22	DDC_CLK
23	GND	24	Back light control
25	GND	26	GND
27	VDD	28	VDD
29	NC	30	VDD

J9 : ATX Power Connector

PIN No.	Signal Description
1	VCC
2	VCC
3	V5SB
4	+V12
5	PS_ON#
6	GND
7	GND
8	GND

J10 : Front Panel Header

PIN No.	Signal Description	PIN No.	Signal Description
1	Buzzer-	2	SUS_LED+
3	NC	4	SUS_LED-
5	NC	6	Power LED-
7	Buzzer+	8	Power LED+
9	Power Bottom+	10	NC
11	Power Bottom-	12	NC
13	Reset+	14	HDD LED+
15	Reset-	16	HDD LED-

Note:
Buzzer :J10-pin 1 and J10-pin 7
Power Button : J10-pin 9 and J10-pin 11
Reset Button : J10-pin 13 and J10-pin 15
SUS_LED:J10-pin 2 and J10-pin 4
Power LED : J10-pin 6 and J10-pin 8
HDD LED : J10-pin 14 and J10-pin 16

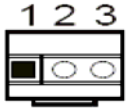
J11/J12 : SATA Connector

PIN No.	Signal Description	
1	GND	GND
2	SATA_TXP0	SATA_TXP3
3	SATA_TXN0	SATA_TXN3
4	GND	GND
5	SATA_RXP0	SATA_RXP3
6	SATA_RXN0	SATA_RXN3
7	GND	GND

J13 : GPIO Header

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO0	2	GPIO5
3	GPIO1	4	GPIO6
5	GPIO2	6	GPIO7
7	GPIO3	8	GPIO8
9	GND	10	VCC

J14 : Fan Connector



PIN No.	Signal Description
1	Ground
2	+12V
3	Fan speed Detecting signal

J15 : PS2 KB/MS Header

PIN No.	Signal Description	PIN No.	Signal Description
1	MS_Data	2	KB_Data
3	NC	4	NC
5	GND	6	GND
7	5V_Dual	8	5V_Dual
9	MS_CLK	10	KB_CLK

J19 : On board COM. Connector

PIN No.	Signal Description
1	DCD (Data Carrier Detect)
2	RXD (Receive Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	GND (Ground)
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)
10	N/C

Chapter 3
System Installation

This chapter provides you with instructions to set up your system. The additional information is enclosed to help you set up onboard PCI device and handle Watch Dog Timer (WDT) and operation of GPIO in software programming.

3.1 Intel® Core 2 Duo (45nm) Small Form Factor (SFF), and Celeron ULV processors

NANO-8050 series built with on-board BGA type INTEL® Core 2 Duo and Celeron ULV processors. Intel® Core 2 Duo processors: SP9300 (2.26GHz), SL9400 (1.86GHz), SU9300 (1.2GHz) & Celeron ULV processors: ULV 722 (1.2GHz), ULV723 (1.2GHz).

3.2 Main Memory

NANO-8050 provides 1 x 200-pin SO-DIMM sockets which supports 800/667 DDR2-SDRAM as main memory, Non-ECC (Error Checking and Correcting), non-register functions. The maximum memory size can be up to 4GB capacity. Memory clock and related settings can be detected by BIOS via SPD interface.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be either one double-sided DIMM in either one DIMM socket or two single-sided SO-DIMM in both sockets.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedures to install memory module into memory socket. Before locking, make sure that all modules have been fully inserted into the card slots.

Note:
To maintain system stability, don't change any of DRAM parameters in BIOS setup to upgrade system performance without acquiring technical information.

Memory frequency / CPU FSB synchronization

NANO-8050 supports different memory frequencies depending on the CPU front side bus and the type of DDR2 SO-DIMM.

CPU FSB	Memory Frequency
1066MHz	800/667MHz
800MHz	800/667MHz

3.3 Installing the Single Board Computer

To install your NANO-8050 into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position
Step 2 : Install and configure CPU and memory module on right position
Step 3 : Place NANO-8050 into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

WARNING

Please ensure that SBC is properly inserted and fixed by mechanism.

Note:
Please refer to section 3.3.1 to 3.3.4 to install INF/VGA/LAN/Audio drivers.

3.3.1 Chipset Component Driver

The chipset on NANO-8050 is a new chipset that a few old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows 2000 /XP, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in NANO-8050 CD-title.

3.3.2 Intel® Integrated Graphics GMCH Chip

Using Intel® GS45 GMCH with Intel® Gen 5.0 integrated graphics engine with 10 integrated chipset is aimed to gain an outstanding graphic performance. This combination makes NANO-8050 an excellent piece of multimedia hardware.

With no additional video adaptor, this onboard video will usually be the system display output. By adjusting the BIOS setting to disable on-board VGA, an add-on PCI-Express by 1 VGA card can take over the system display.

Drivers Support

Please find Springdale GMCH driver in the NANO-8050 CD-title. Drivers support Windows-2000, Windows XP.

3.3.3 Intel® Gigabit Ethernet Controller

Drivers Support

Please find Intel® 82567LM LAN (J6) driver in /Ethernet directory of NANO-8050 CD-title. The drivers support Windows 2000 /XP / Server 2003.

LED Indicator (for LAN status)

NANO-8050 provides two LED indicators to report Intel® 82567LM Gigabit Ethernet interface status. Please refer to the table below as a quick reference guide.

8111C	Color	Name of LED	Operation of Ethernet Port		
			Linked	Active	
Status LED	Orange	LAN Linked & Active LED	On	Blinking	
Speed LED	Orange	LAN speed LED	Giga Mbps	100 Mbps	10 Mbps
	Green		Orange	Green	Off

3.3.4 Audio Controller

Please find Realtek ALC262 Audio driver form NANO-8050 CD-title. The drivers support Windows 2000 /XP.

3.4 Clear CMOS Operation

The following table indicates how to enable/disable Clear CMOS Function hardware circuit by putting jumpers at proper position.

JP5 : RTC Reset

JP5	Function
1-2 Short	Normal Operation ★
2-3 Short	Clear CMOS

3.5 WDT Function

The working algorithm of the WDT function can be simply described as a counting process. The time-out interval can be set through software programming. The availability of the time-out interval settings by software or hardware varies from boards to boards.

NANO-8050 allows user control WDT through dynamic software programming. The WDT starts counting when it is activated. It sends out a signal to system reset or to non-maskable interrupt (NMI), when time-out interval ends. To prevent the time-out interval from running out, a re-trigger signal will need to be sent before the counting reaches its end. This action will restart the counting process. A well-written WDT program should keep the counting process running under normal condition. WDT should never generate a system reset or NMI signal unless the system runs into troubles.

The related control registers of WDT are all included in the following sample program that is written in C language. User can fill a non-zero value into the time-out value register to enable /refresh WDT. System will be reset after the time-out value to be counted down to zero. Or user can directly fill a zero value into time-out value register to disable WDT immediately. To ensure accessing to the content of desired control register, the sequence of following program codes should be step-by-step run again when each register is accessed. Additionally, there are maximum 2 seconds of counting tolerance that should be considered into user application program. For more information about WDT, please refer to Winbound W83627THG data sheet.

There are two PNP I/O port addresses that can be used to configure WDT,
1) 0x2E:EEIR (Extended Function Index Register, for identifying CR index number)
2) 0x2F:EFDR (Extended Function Data Register, for accessing desired CR)

Below are some example codes, which demonstrate the use of WDT.

```
// Enter Extended Function Mode
outp(0x002E, 0x87);
outp(0x002E, 0x87);
// Assign Pin 89to be a WDTO
outp(0x002E, 0x2B);
outp(0x002F, inp(0x002F) & 0XEF);
// Select Logic Device 8
outp(0x002E, 0x07);
outp(0x002F, 0x08);
// Active Logic Device 8
outp(0x002E, 0X30);
outp(0x002F, 0x01);
```

```
// Select Count Mode
 outp(0x002E, 0xF5);
 outp(0x002F, (inp(0x002F) & 0xF7) |(Count-mode Register & 0x08));
// Specify Time-out Value
 outp(0x002E, 0XF6);
 outp(0x002F, Time-out Value Register);
// Disable WDT reset by keyboard / mouse interrupts
 outp(0x002E, 0xF7);
 outp(0x002F, 0x00);
// Exit Extended Function Mode
outp(0x002E, 0xAA);
```

Definitions of Variables:

Value of Count-mode Register:
1) 0x00 – Count down in seconds (Bit3=0)
2) 0x08 – Count down in minutes (Bit3=1)

Value of Time-out Value Register:
1) 0x00 – Time-out Disable
2) 0x01~0xFF –Value for counting down

3.6 GPIO

The NANO-8050 provides 8 programmable input or output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O selection. To invert port value, the setting of inversion register has to be made. Port values can be set to read or write through data register.

3.6.1 Pin assignment

J8 : General Purpose I/O Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	General Purpose I/O Port 0 (GPIO0)	2	General Purpose I/O Port 4 (GPIO4)
3	General Purpose I/O Port 1 (GPIO1)	4	General Purpose I/O Port 5 (GPIO5)
5	General Purpose I/O Port 2 (GPIO2)	6	General Purpose I/O Port 6 (GPIO6)
7	General Purpose I/O Port 3 (GPIO3)	8	General Purpose I/O Port 7 (GPIO7)
9	Ground	10	+5V

3.6.2 NANO-8050 GPIO Programming Guide

There are 8GPIO pins on NANO-8050 series. There are GPIO pins from SUPER I/O (W83627THG) GPIO pins, and can be programmed as Input or Output direction.

J13 pin header is for 8GPIO pins and its pin assignment as following :

J13_Pin1=GPIO1:from SUPER I/O_GPIO10 with Ext. 4.7K PH
J13_Pin3=GPIO2:from SUPER I/O_GPIO11 with Ext. 4.7K PH
J13_Pin5=GPIO3:from SUPER I/O_GPIO12 with Ext. 4.7K PH
J13_Pin7=GPIO4:from SUPER I/O_GPIO13 with Ext. 4.7K PH
J13_Pin2=GPIO5:from SUPER I/O_GPIO15 with Ext. 4.7K PH
J13_Pin4=GPIO6:from SUPER I/O_GPIO16 with Ext. 4.7K PH
J13_Pin6=GPIO7:from SUPER I/O_GPIO17 with Ext. 4.7K PH
J13_Pin8=GPIO8:from SUPER I/O_GPIO18 with Ext. 4.7K PH

<<<<< Be careful Pin9=GND , Pin10=VCC >>>>>

There are several Configuration Registers (CR) of W83627THG needed to be programmed to control the GPIO direction, and status (GPI)/value (GPO). CR00h~CR2F are common (global) registers to all Logical Devices (LD) in W83627THG. CR07h contains the Logical Device Number that can be changed to access the LD as needed. LD7 contains the GPIO10~17 registers.

Chapter 4
BIOS Setup Information

NANO-8050 is equipped with the AMI BIOS stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, NANO-8050 communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

4.1 Entering Setup -- Launch System Setup

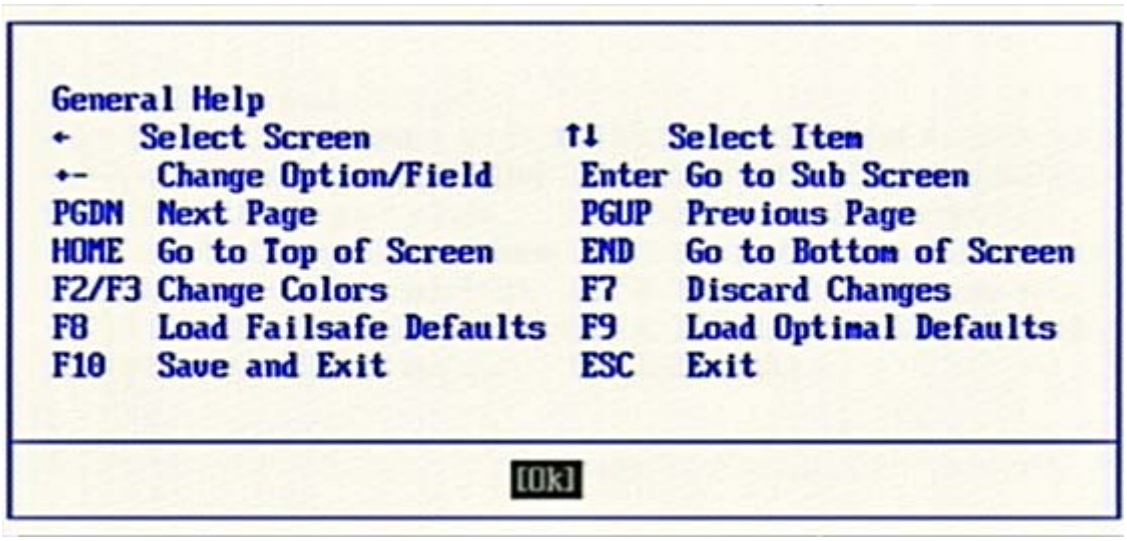
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <Del> key to enter Setup.

Press <Del> to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system by turning it OFF and On or pressing the RESET button. You may also restart the system by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys.

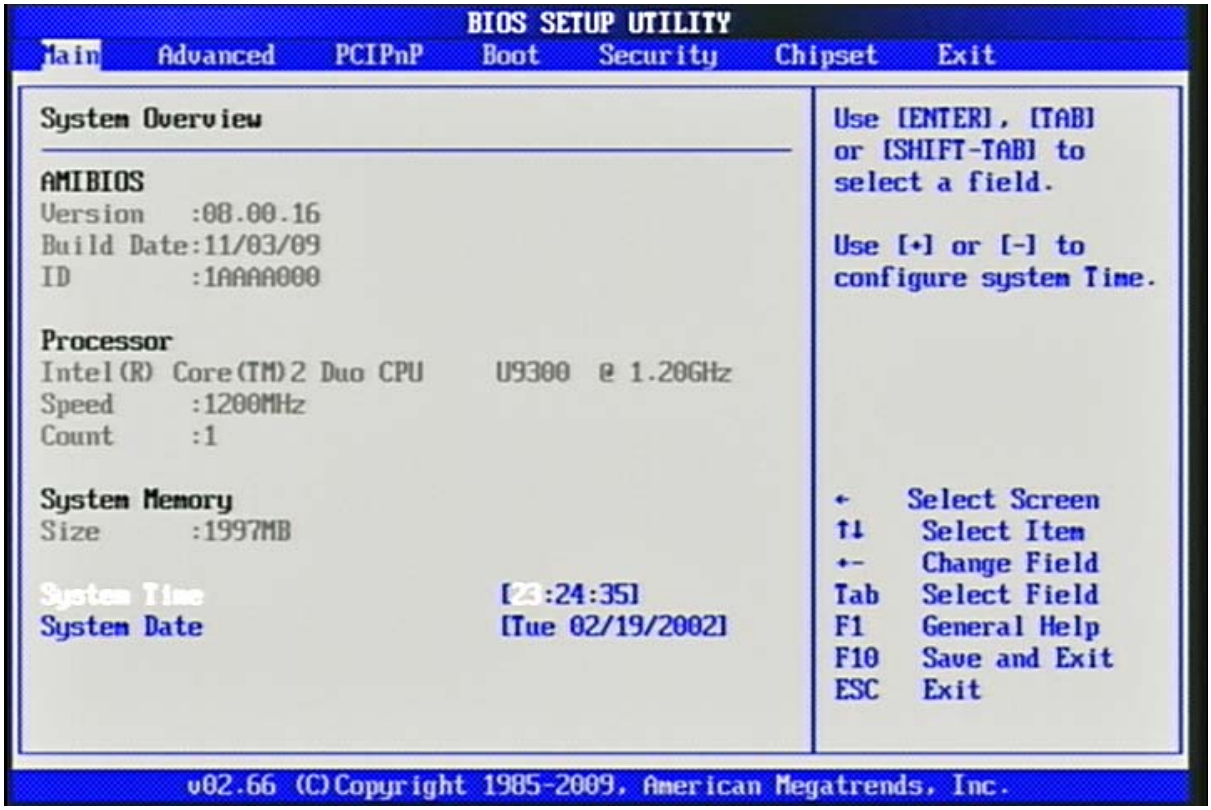
Press <F1> to Run SETUP or Resume

The BIOS setup program provides a General Help screen. You can call up this screen from any menu by simply pressing <F1>. The Help screen lists the appropriate keys to use and the possible selections for the highlighted item. Press <Esc> to exit the Help screen.



4.2 Main

Use this menu for basic system configurations, such as time, date etc.



AMI BIOS, Processor, System Memory

These items show the firmware and hardware specifications of your system. Read only.

System Time

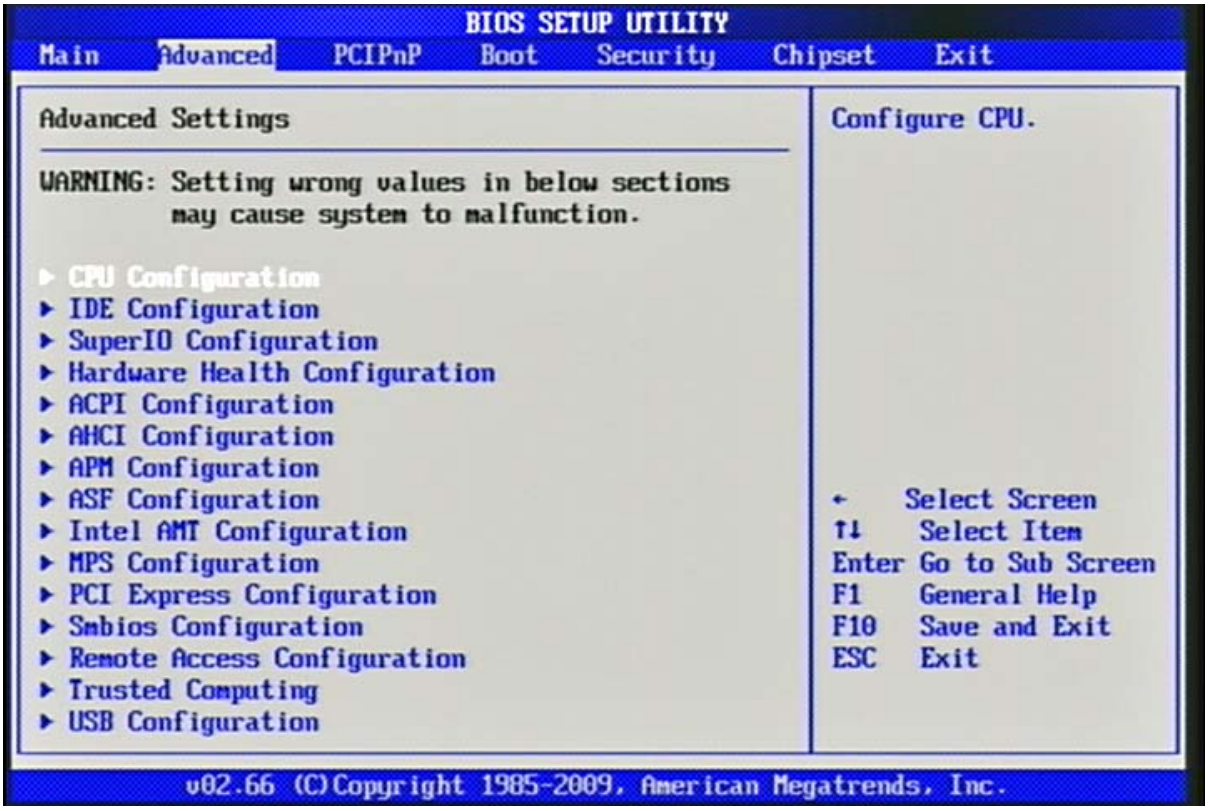
The time format is <Hour> <Minute> <Second>. Use [+] or [−] to configure system Time.

System Date

The date format is <Day>, <Month> <Date> <Year>. Use [+] or [−] to configure system Date.

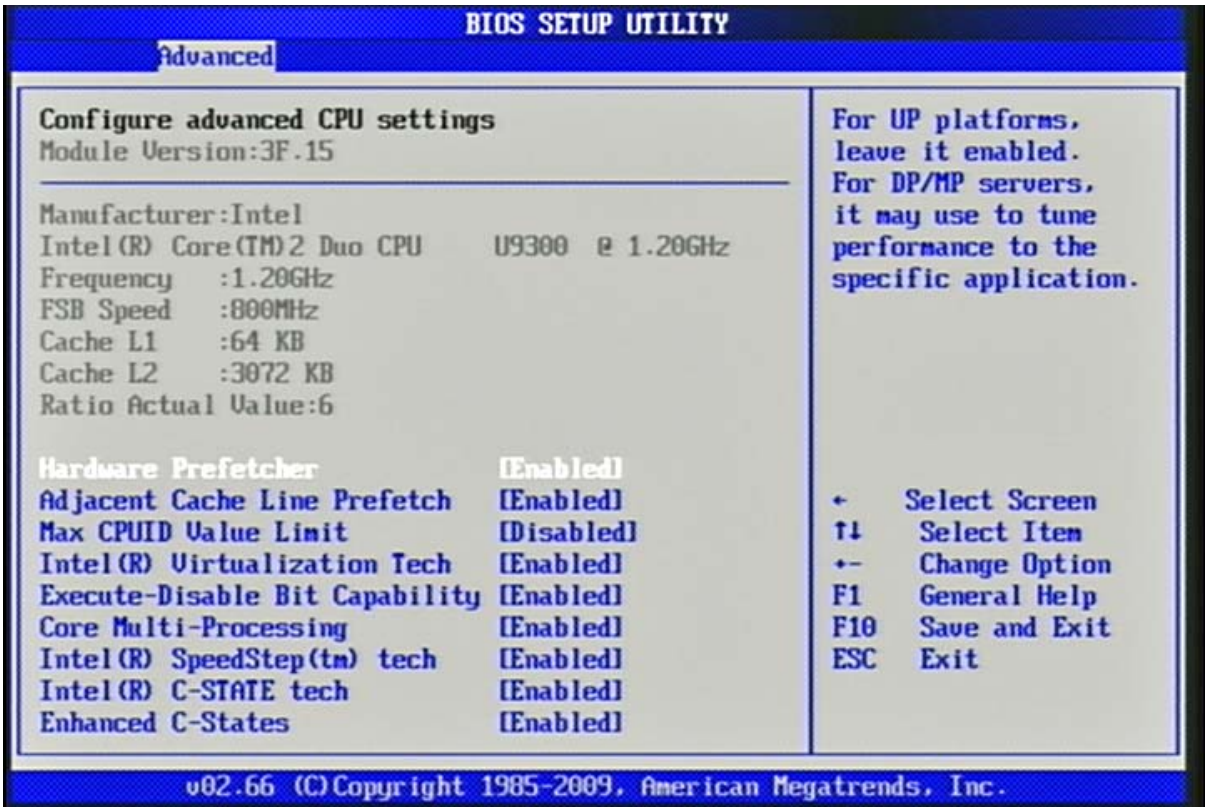
4.3 Advanced

Use this menu to set up the items of special enhanced features.



CPU Configuration

These items show the advanced specifications of your CPU. Read only.


BIOS SETUP UTILITY
Advanced
Configure advanced CPU settings
Module Version:3F.15
Manufacturer:Intel
Intel(R) Core(TM)2 Duo CPU U9300 @ 1.20GHz
Frequency :1.20GHz
FSB Speed :800MHz
Cache L1 :64 KB
Cache L2 :3072 KB
Ratio Actual Value:6
Hardware Prefetcher [Enabled]
Adjacent Cache Line Prefetch [Enabled]
Max CPUID Value Limit [Disabled]
Intel(R) Virtualization Tech [Enabled]
Execute-Disable Bit Capability [Enabled]
Core Multi-Processing [Enabled]
Intel(R) SpeedStep(tm) tech [Enabled]
Intel(R) C-STATE tech [Enabled]
Enhanced C-States [Enabled]
For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance to the specific application.
← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
v02.66 (C)Copyright 1985-2009, American Megatrends, Inc.

Hardware Prefetcher

For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance the specific application.

The choice: Disabled, Enabled.

Adjacent Cache Line Prefetch

For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance the specific application.

The choice: Disabled, Enabled.

Max CPUID Value Limit

Disabled for Windows XP

The choice: Disabled, Enabled.

Intel® Virtualization Tech

A VMM can utilize the additional HW Caps, provided by Intel® Virtualization Tech.

Note: A full reset is required to change the setting.
The choice: Disabled, Enabled.

Execute-Disable Bit capability

When disabled, force the XD feature flag to always return 0

The choice: Disabled, Enabled.

Core Multi-Processing

Disabled disable one execution core of each CPU die.

The choice: Disabled, Enabled.

Intel® Speed Step (tm) Tech

Disable: Disable GV3.
Enable: Enable GV3.

Intel® C-STATE Tech

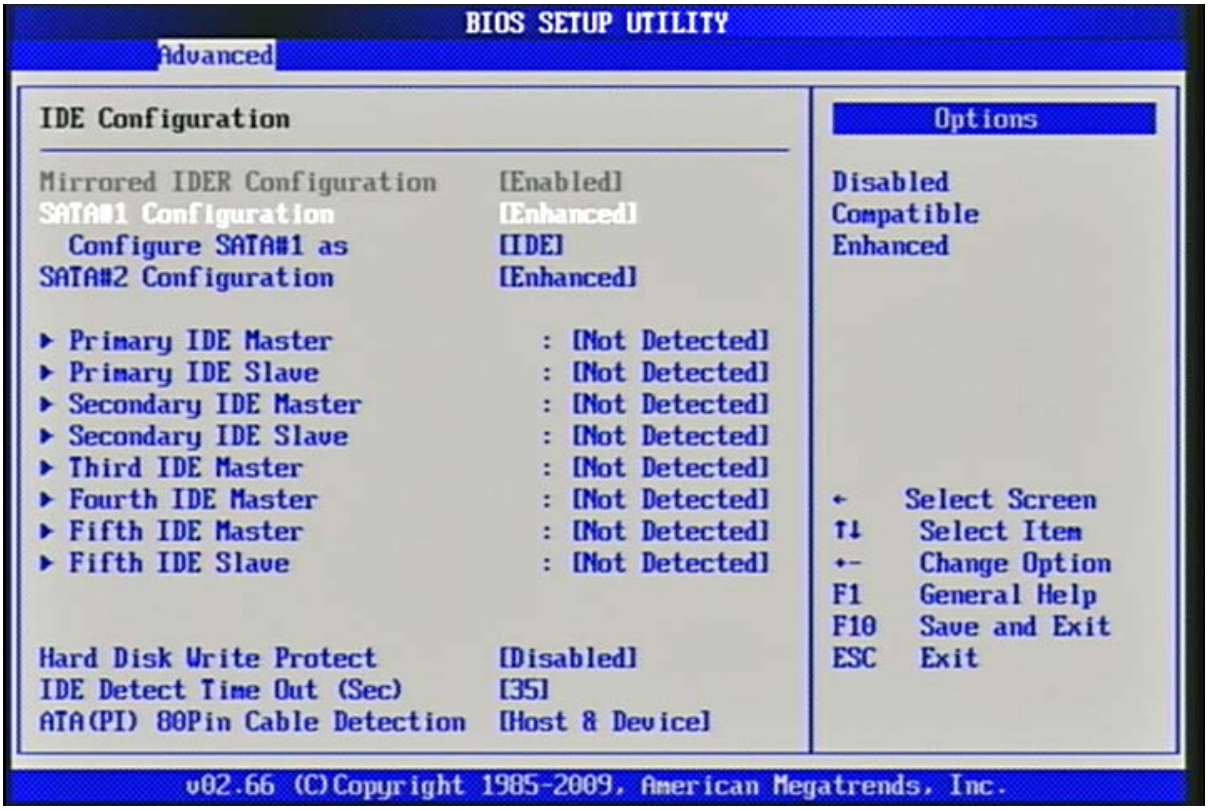
CPU idle is set to C2, C3, C4 State.

Enhanced C-States

CPU idle is set to Enhanced C-States.

IDE Configuration

The IDE Configuration the IDE devices, such as hard disk drive or CD-ROM drive. It uses a separate sub menu to configure each hard disk drive (Master and Slave).



Mirrored IDER Configuration

The choice: Disabled, Enabled.

SATA#1 Configuration

The choice: Disabled, Compatible, Enabled.

Configure SATA#1 as

This setting specifies the function of the on-chip SATA#1 controller.

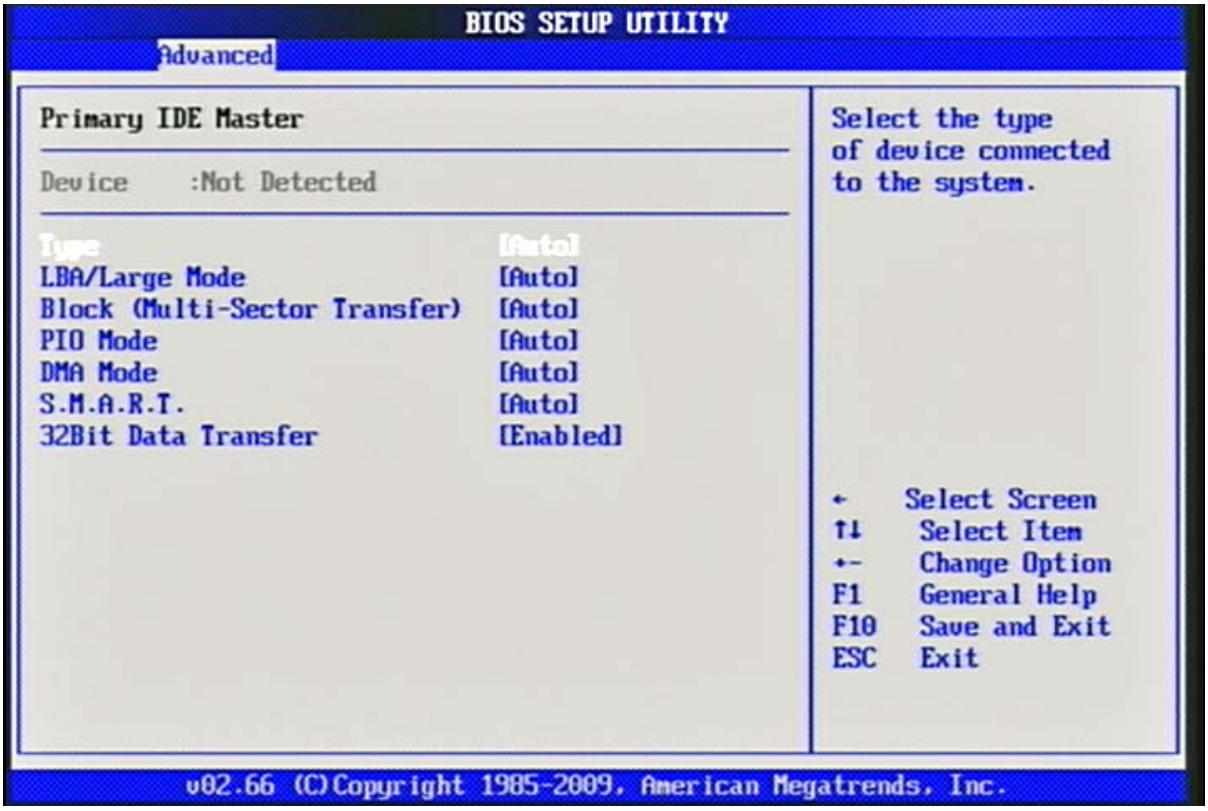
The choice: IDE, RAID, AHCI.

SATA#2 Configuration

The choice: Disabled, Enabled.

Primary / Secondary / Third / Fourth /Fifth IDE Master / Slave

While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto detection of IDE devices.



[Type] Press PgUp/<+> or PgDn/<—> to select [Manual], [None] or [Auto] type. You can use [Manual] to define your own drive type manually.

[LBA/Large Mode] Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads and Sectors.

[Block (Multi-Sector Transfer)] Any selection except Disabled determines the number of sectors transferred per block.

[PIO Mode] Indicates the type of PIO (Programmed Input/Output)

[DMA Mode] Indicates the type of Ultra DMA

[S.M.A.R.T.] This allows you to activate the S.M.A.R.T. (Self-Monitoring Analysis & Reporting Technology) capability for the hard disks. S. M.A.R.T is a utility that monitors your disk status to predict hard disk failure. This gives you an opportunity to move data from a hard disk that is going to fail to a safe place before the hard disk becomes offline.

[32 Bit Data Transfer] Enable/Disable 32-bit Data Transfer.

Hard Disk Write Protect

Disabled/Enabled device write protection, this will be effective only if device is accessed through BIOS.

The choice: Disabled, Enabled.

IDE Detect Time Out (Sec)

Select the time out value for detecting ATA/ATAPI device (s).

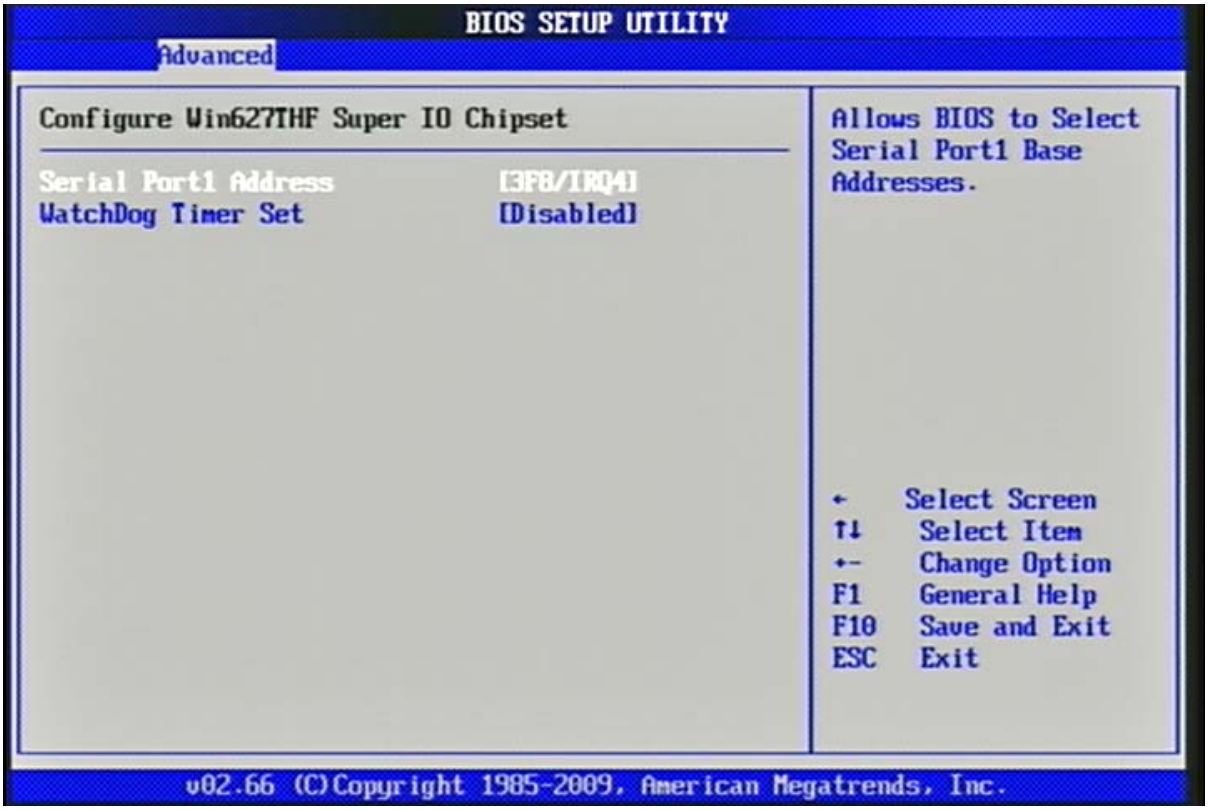
The choice: 0, 5, 10, 15, 20, 25, 30, 35.

ATA(PI) 80Pin Cable Detection

Select the mechanism for detecting 80Pin ATA (PI) cable.

The choice: Host & Device, Host, Device.

Super IO Configuration



Serial Port 1 Address

Allows BIOS Select Serial Port1 Base Addresses.

The choice: Disabled, 3F8/IRQ4, 3E8/IRQ4, 2E8/IRQ3.

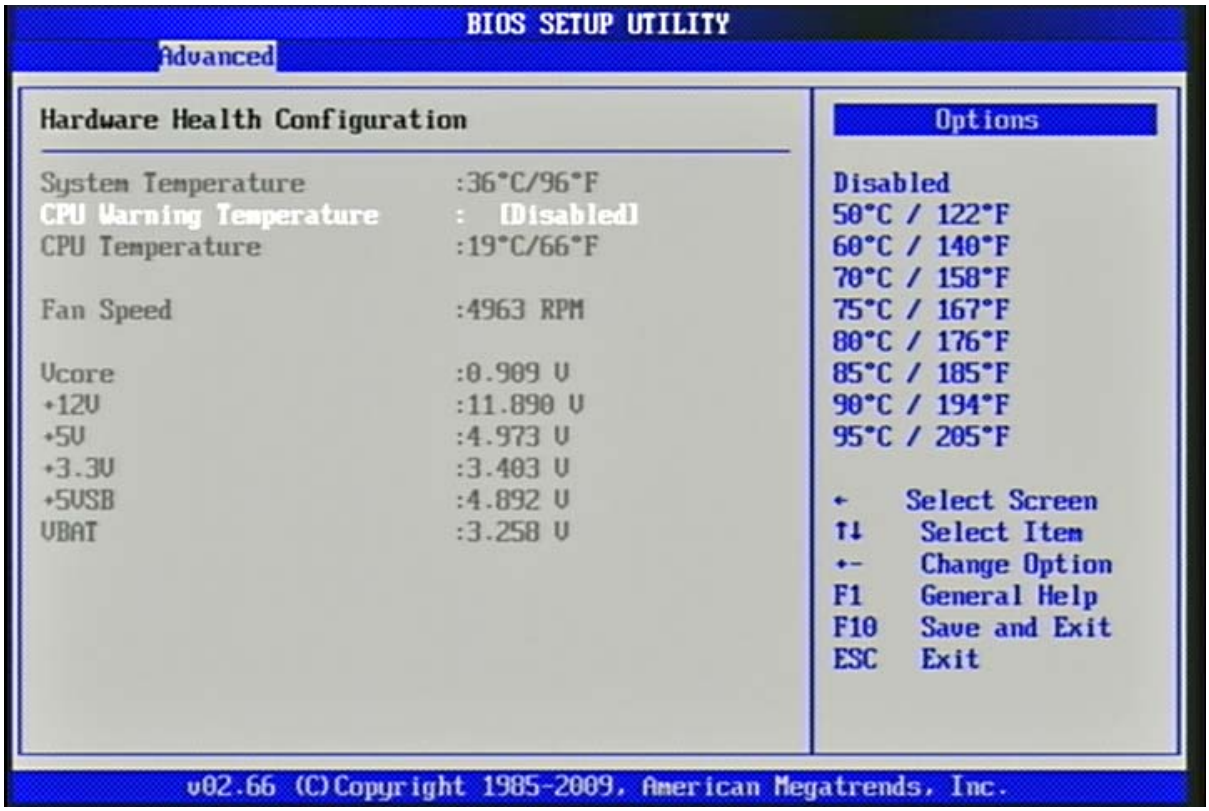
Watch Dog Timer Set

This BIOS testing option is able to reset the system according to the selected table.

The choice: Disabled, 10, 20, 30, 40 sec. 1, 2, 4 min.

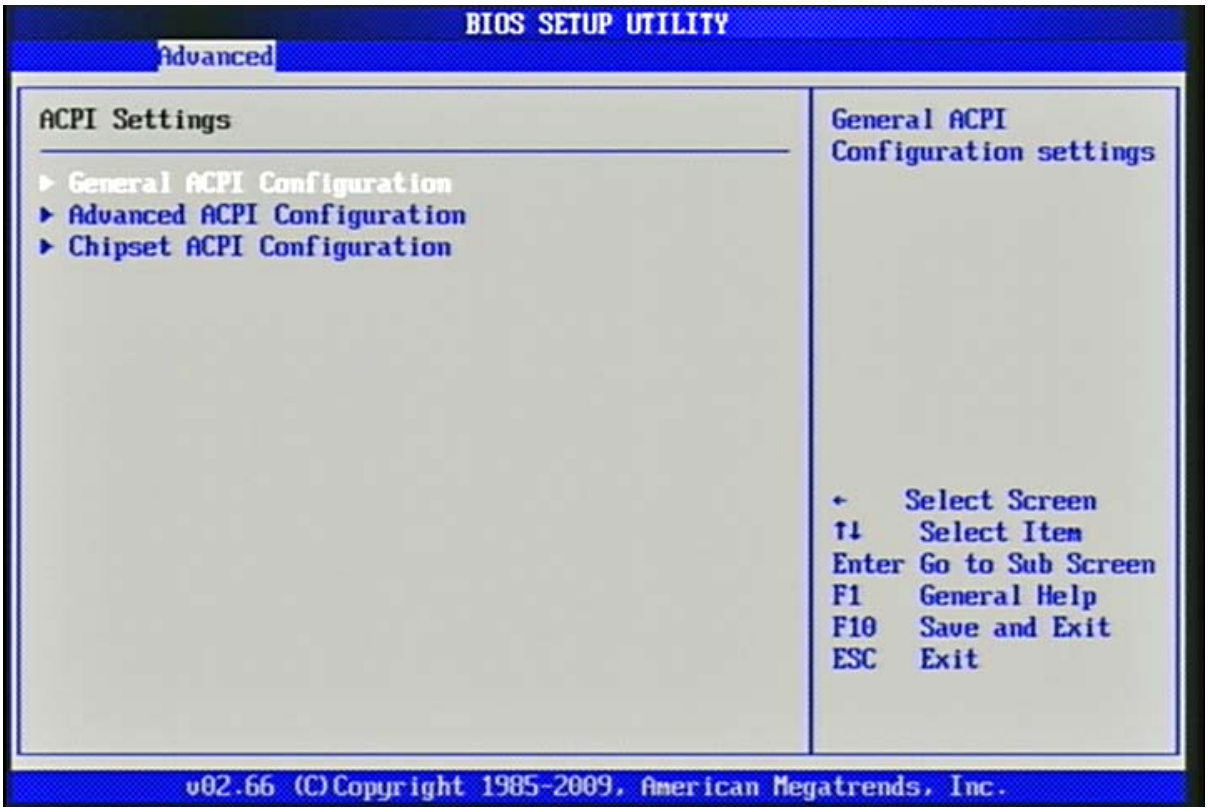
Hardware Health Configuration

Configuration / monitor the Hardware Health.

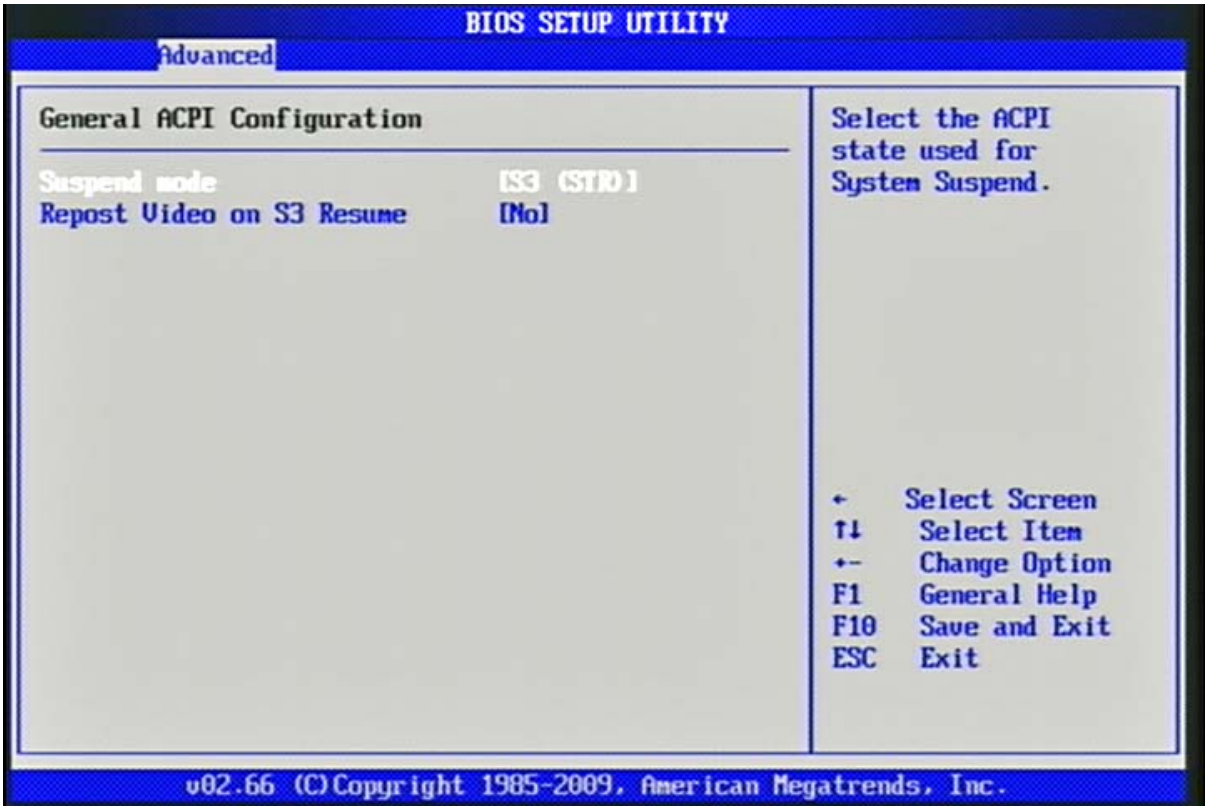


ACPI Settings

Select for Advanced ACPI Configuration.



General ACPI Configuration



Suspend mode

This item specifies the power saving modes for ACPI function. If your operating system supports ACPI, you can choose to enter the Standby mode in S1 (POS) or S3 (STR) fashion through the setting of this field. Options are:

[S1 (POS)] The S1 sleep mode is a low power state. In this state, no system context is lost (CPU or chipset) and hardware maintains all system contexts.

[S3 (STR)] The S3 sleep mode is a lower power state where the information of system configuration and open applications/ files is saved to main memory that remains powered while most other hardware components turn off to save energy. The information stored in memory will be used to restore the system when a "wake up" event occurs.

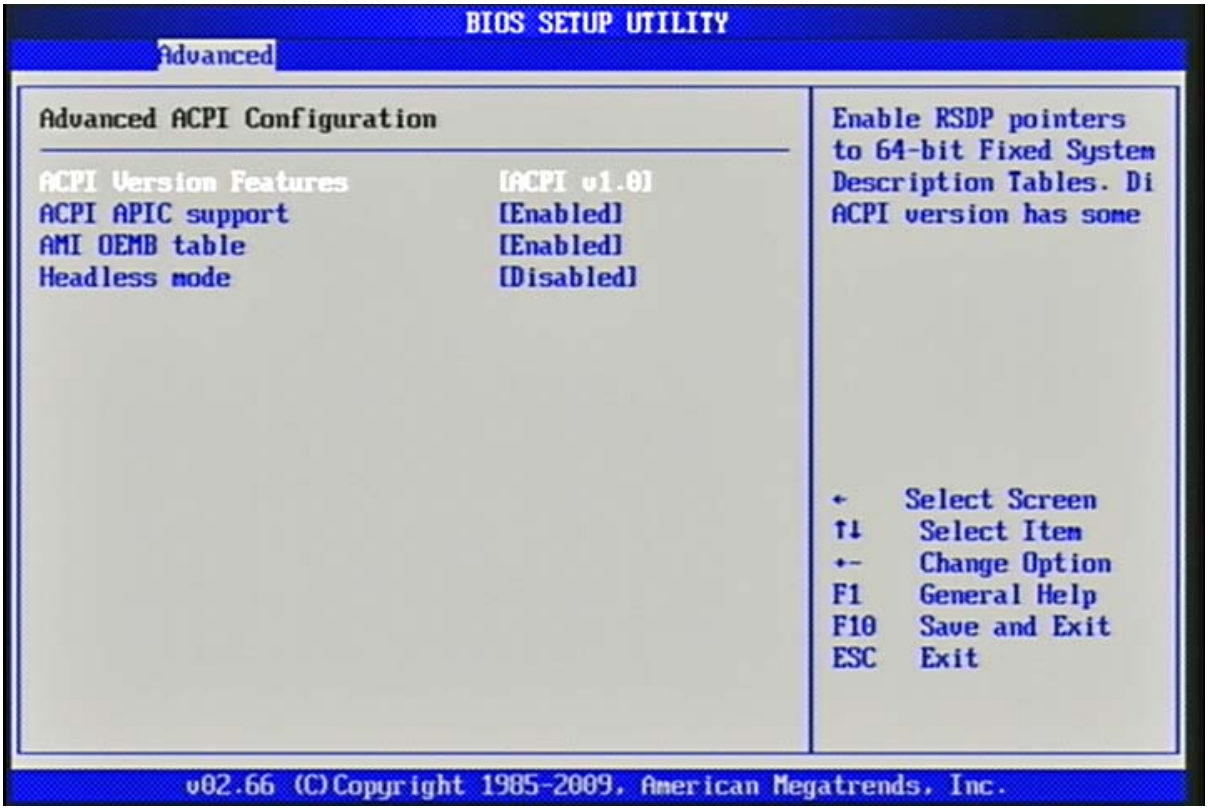
Repost Video on S3 Resume

Determines whether to invoke VGA BIOS post on S3/STR resume.

The choice: No, Yes

Advanced ACPI Configuration

Advanced ACPI Configuration settings, Use this section to configure additional ACPI options.


BIOS SETUP UTILITY
Advanced
Advanced ACPI Configuration
ACPI Version Features [ACPI v1.0]
ACPI APIC support [Enabled]
AMI OEMB table [Enabled]
Headless mode [Disabled]
Enable RSDP pointers to 64-bit Fixed System Description Tables. Di ACPI version has some
← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
v02.66 (C)Copyright 1985-2009, American Megatrends, Inc.

ACPI Version Features

Enable RSDP pointers to 64-bit Fixed System Description Tables.

The choice: ACPI v1.0 / ACPI v2.0 / ACPI v3.0.

ACPI APIC support

Include ACPI APIC table pointer to RSDT pointer list.

The choice: Disabled, Enabled.

AMI OEMB table

Include OEMB table pointer to R(X) SDT pointer list.

The choice: Disabled, Enabled.

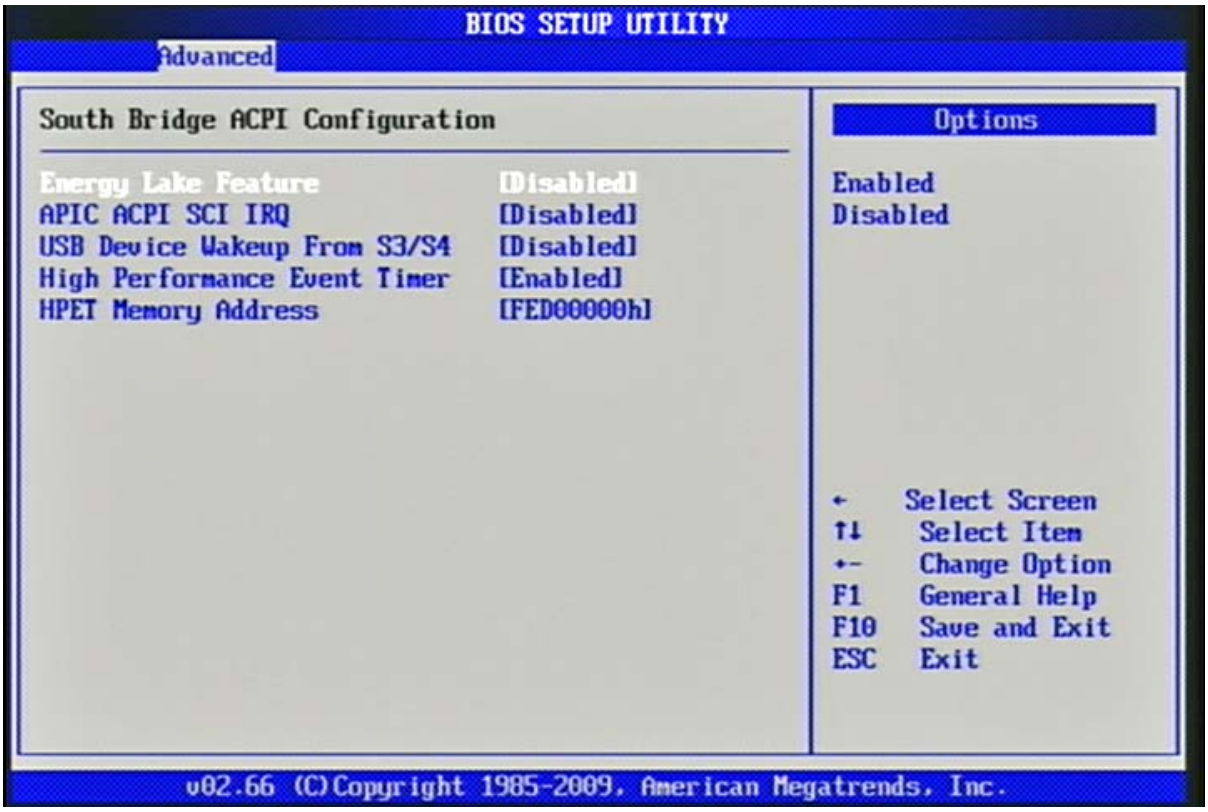
Headless mode

Enable / Disable Headless operation mode through ACPI.

The choice: Disabled, Enabled.

South Bridge ACPI Configuration

The South Bridge ACPI related Configuration settings, Use this section to configure additional ACPI options.



Energy Lake Feature

Select the ACPI state used for System Suspend.

The choice: Disabled, Enabled.

APIC ACPI SCI IRQ

Enable / Disable APIC ACPI SCI IRQ.

The choice: Disabled, Enabled.

USB Device Wakeup From S3/S4

Enable / Disable USB device Wake from S3/S4 mode.

The choice: Disabled, Enabled.

High Performance Event Timer

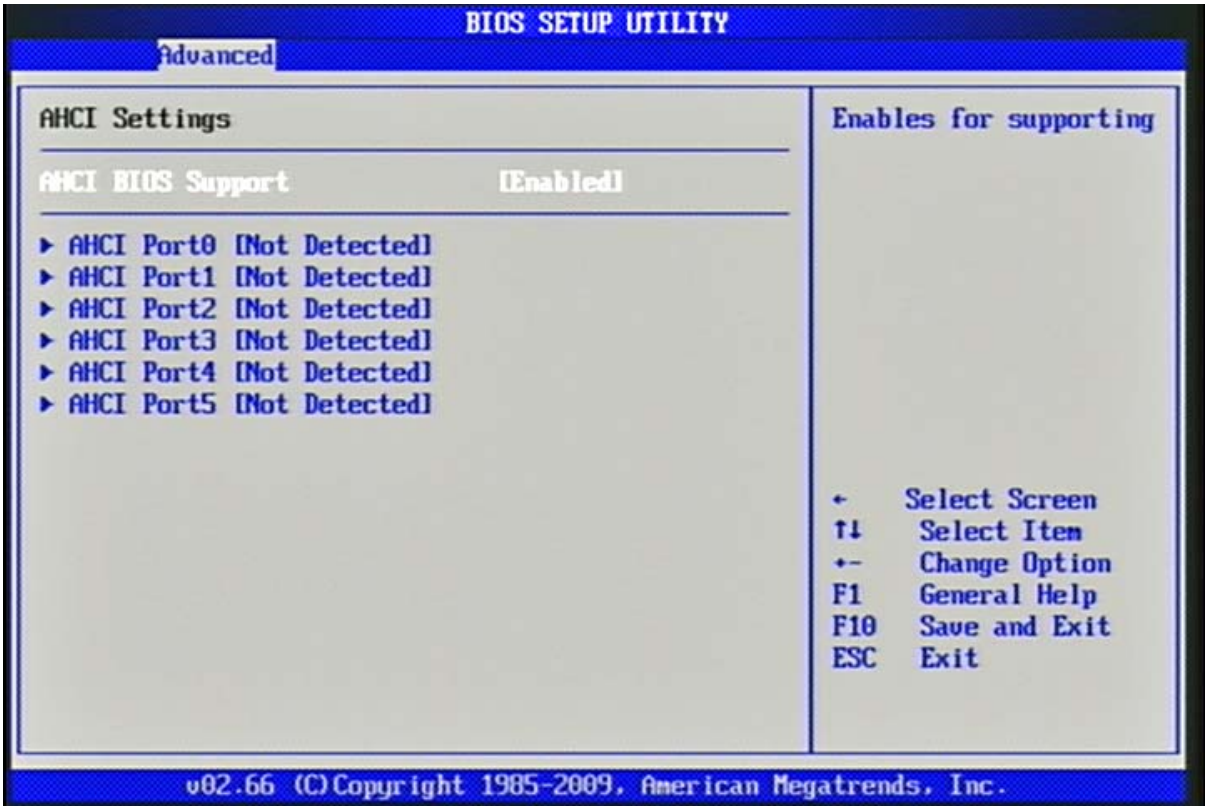
The choice: Disabled, Enabled.

HPET Memory Address

The choice: FED0000h, FED1000h, FED2000h, FED3000h

AHCI Settings

Select for AHCI Configuration.



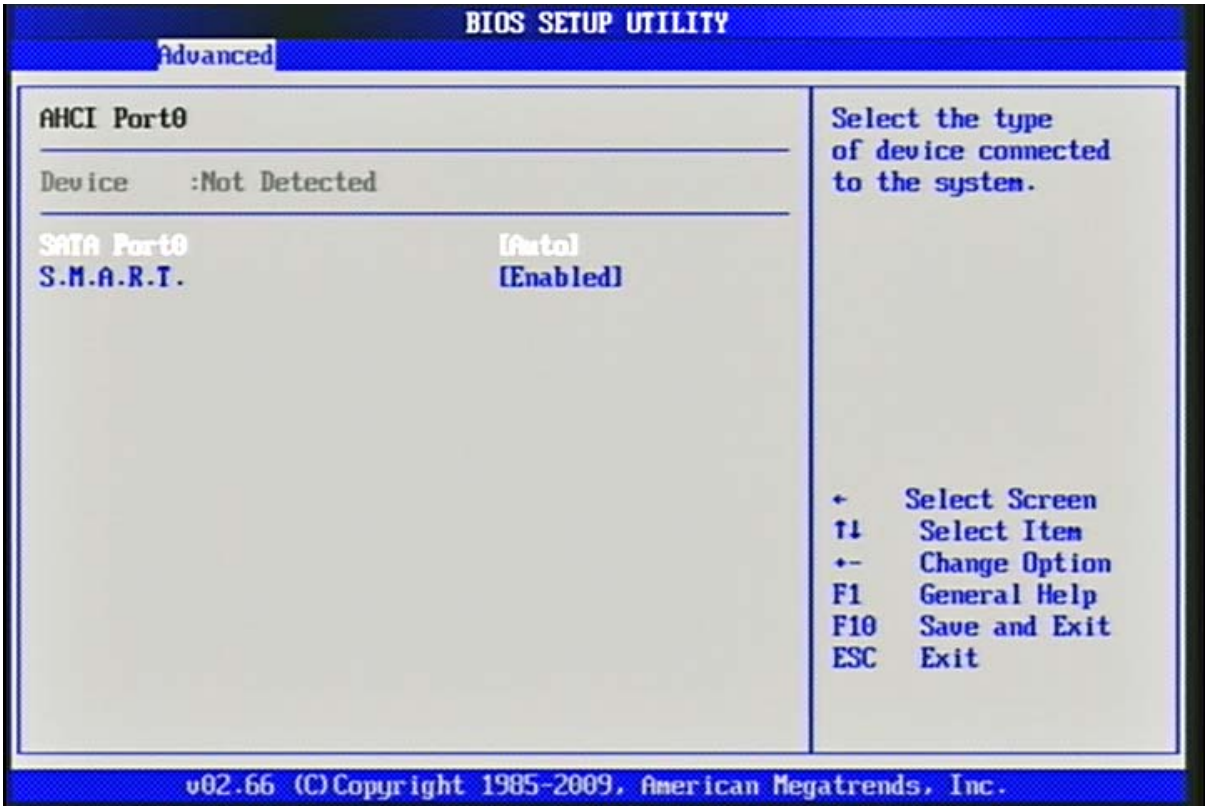
AHCI BIOS Support

Enables for supporting

The choice: Disabled, Enabled.

AHCI Port0 ~ Port5

While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto detection of IDE devices.



SATA Port0 ~ Port5

Select the type of device connected to the system.

The choice: Auto, Not Installed.

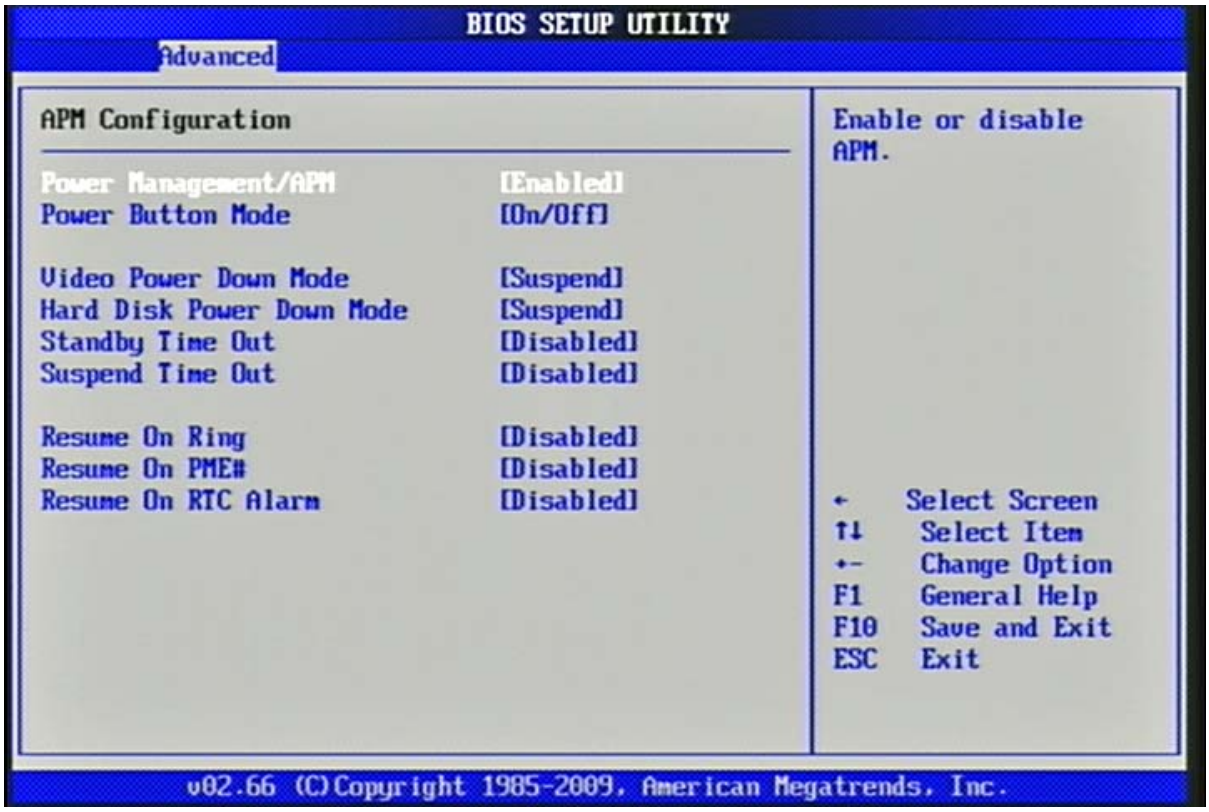
S.M.A.R.T

This allows you to activate the S.M.A.R.T. (Self-Monitoring Analysis & Reporting Technology) capability for the hard disks. S. M.A.R.T is a utility that monitors your disk status to predict hard disk failure. This gives you an opportunity to move data from a hard disk that is going to fail to a safe place before the hard disk becomes offline.

The choice: Disabled, Enabled.

APM Configuration

Select for APM Configuration.



Power Management/APM

Enables for Power Management.

The choice: Disabled, Enabled.

Power Button Mode

Go into On/Off or Suspend when Power button is pressed.

The choice: On/Off, Suspend.

Video Power Down Mode

Power Down video in Suspend or Standby mode.

The choice: Disable, Standby, Suspend.

Hard Disk Power Down Mode

Power Down Hard Disk in Suspend or Standby mode.

The choice: Disable, Standby, Suspend.

Standby Time out

Go into Standby in the specified Time.

The choice: Disable. 1 Min, 2 Min, 4 Min, 8 Min, 10 Min, 20 Min, 30 Min, 40 Min, 50 Min, 60 Min.

Suspend Time out

Go into Suspend in the specified Time.

The choice: Disable. 1 Min, 2 Min, 4 Min, 8 Min, 10 Min, 20 Min, 30 Min, 40 Min, 50 Min, 60 Min.

Resume On Ring

The choice: Disabled, Enabled.

Resume On PME#

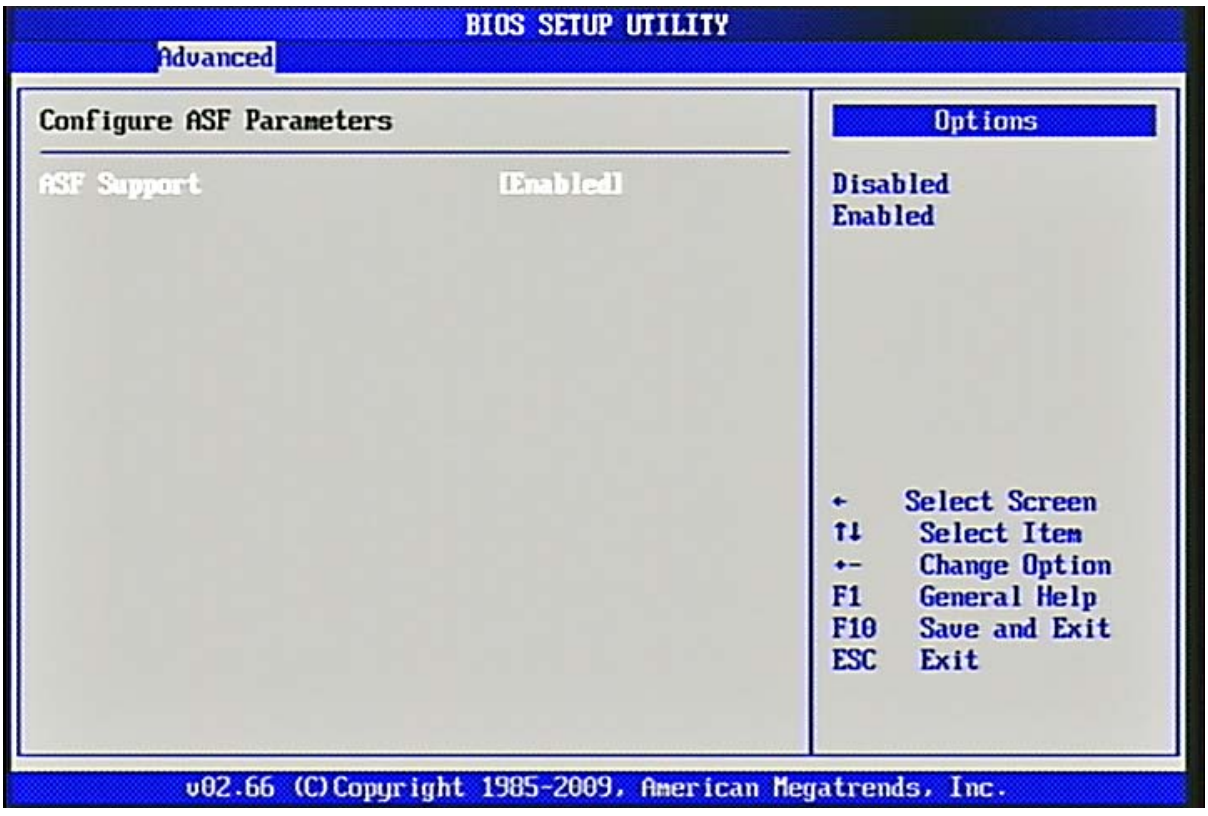
The choice: Disabled, Enabled.

Resume On RTC Alarm

The choice: Disabled, Enabled.

Configure ASF Parameters

Select for ASF Support

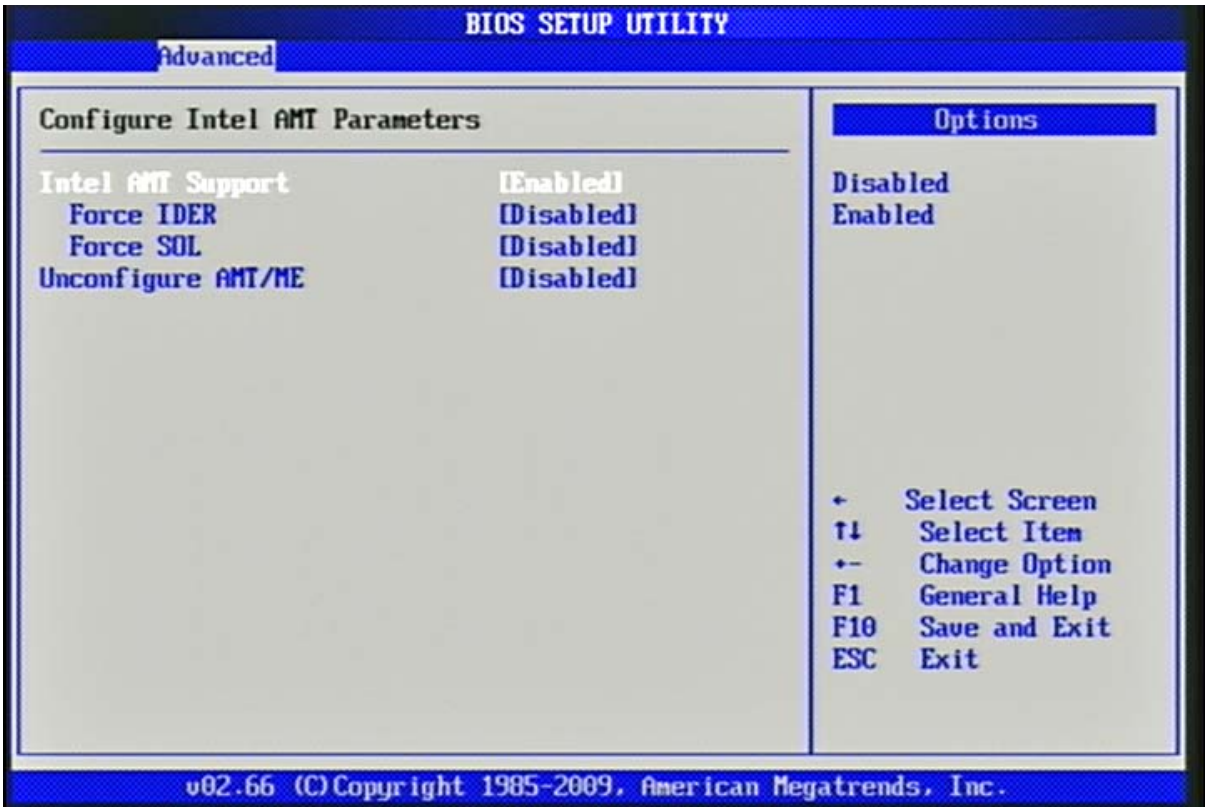


ASF Support

The choice: Disabled, Enabled.

Configure Intel® AMT Parameters

Select for Intel® AMT Configuration.



Intel® AMT Support

The choice: Disabled, Enabled.

Force IDER

The choice: Disabled, IDER Pri. Master, IDER Pri. Slave, IDER Sec. Master, IDER Sec. Slave

Force SOL

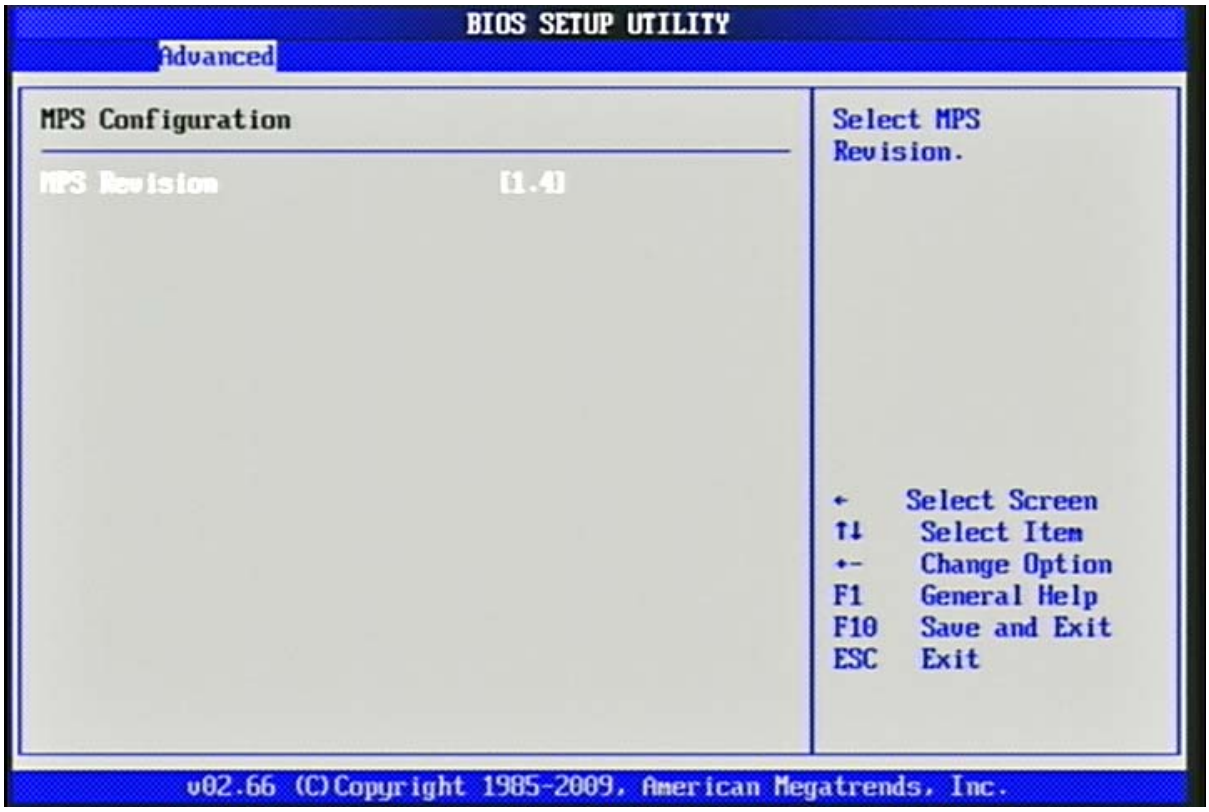
The choice: Disabled, Enabled.

Unconfigure AMT/ME

The choice: Disabled, Enabled.

MPS Configuration

Configure the Multi-Processor Table.



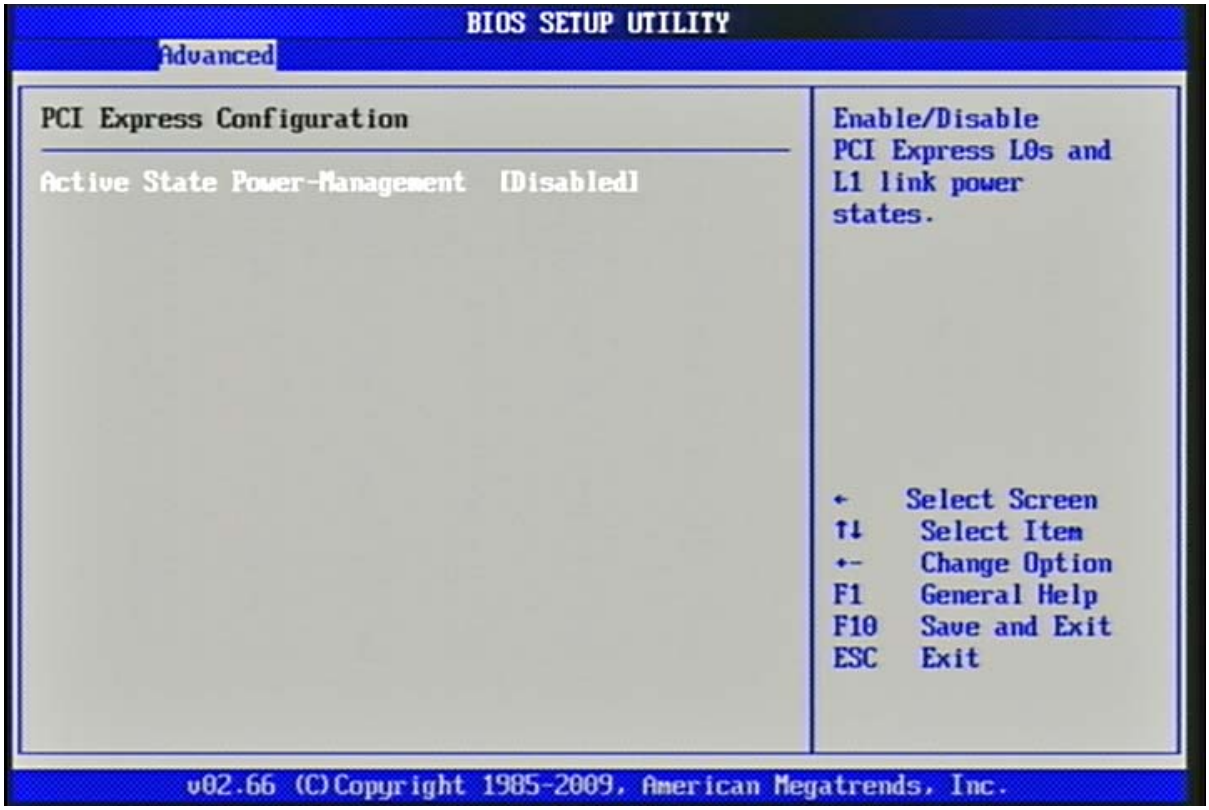
MPS Revision

This field allows you to select which MPS (Multi-Processor Specification) version to be used for the operating system. You need to select the MPS version supported by your operating system. To find out which version to use, consult the vendor of your operating system.

The choice: 1.1, 1.4.

PCI Express Configuration

Configure PCI Express Support.



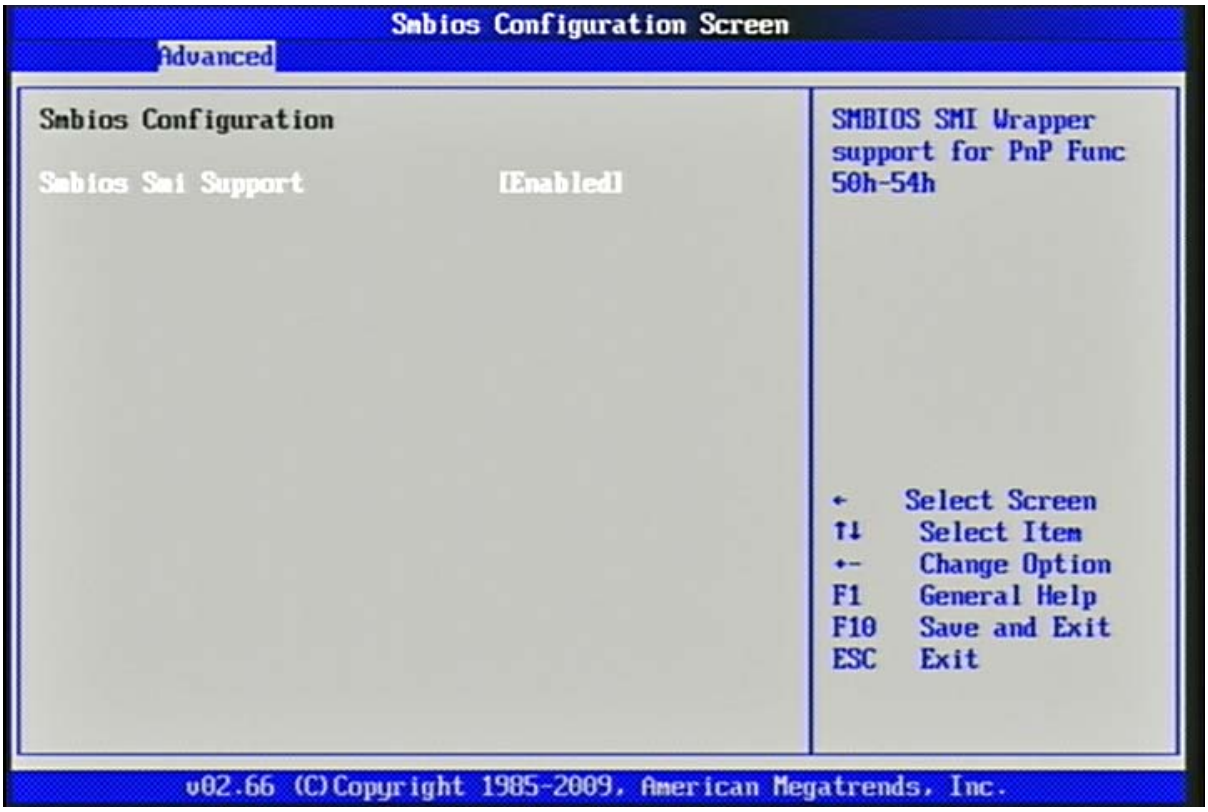
Active State Power-Management

PCI Express L0s and L1 link power states.

The choice: Disabled, Enabled.

Smbios Configuration

SMBIOS Configuration Menu

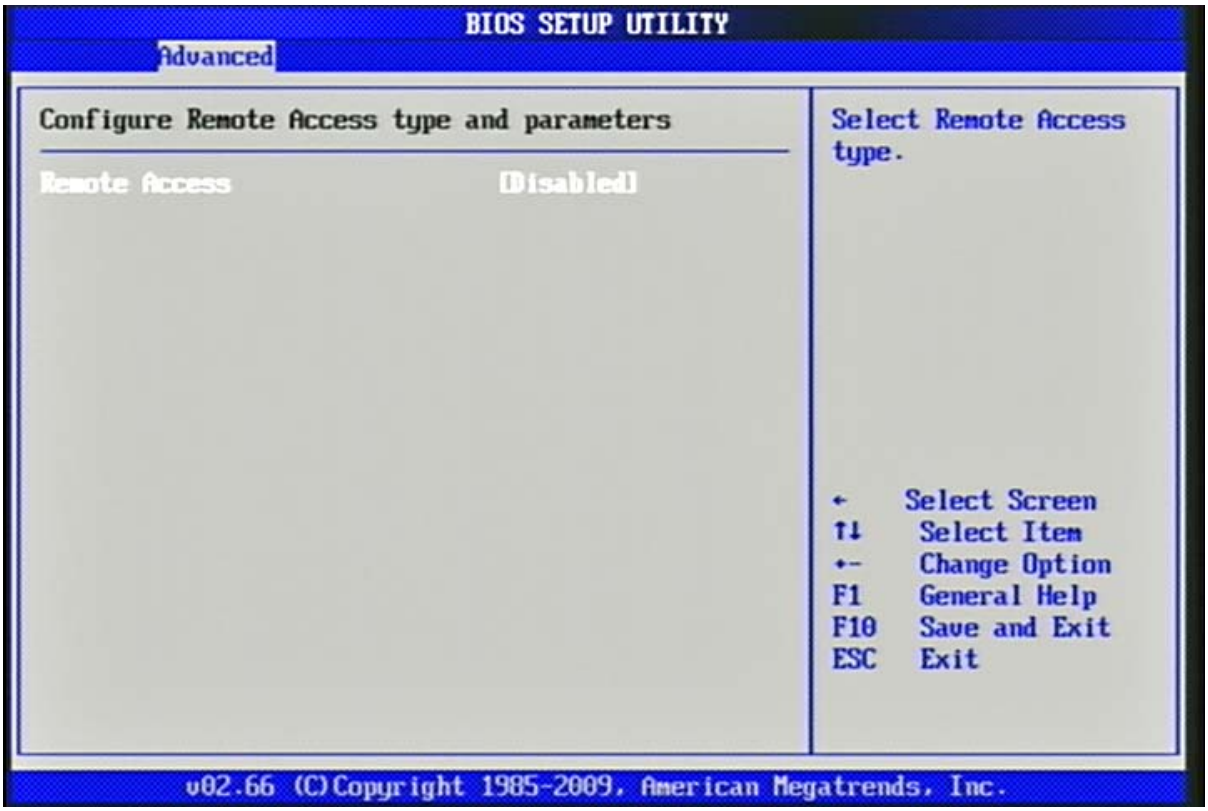


Smbios Smi Support

SMBIOS SMI Wrapper support for PnP Function 50h-54h

The choice: Disabled, Enabled.

Configure Remote Access type and parameters

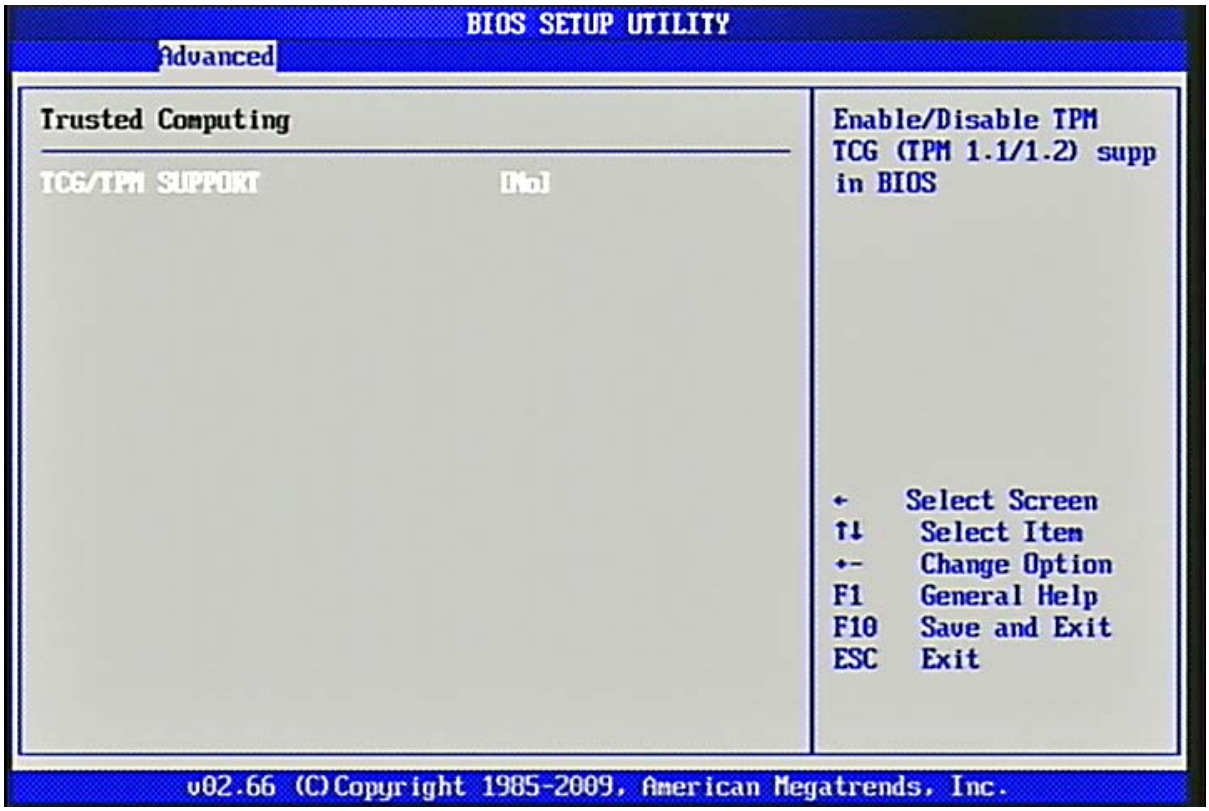


Remote Access

Select Remote Access type.

The choice: Disabled, Enabled.

Trusted Computing

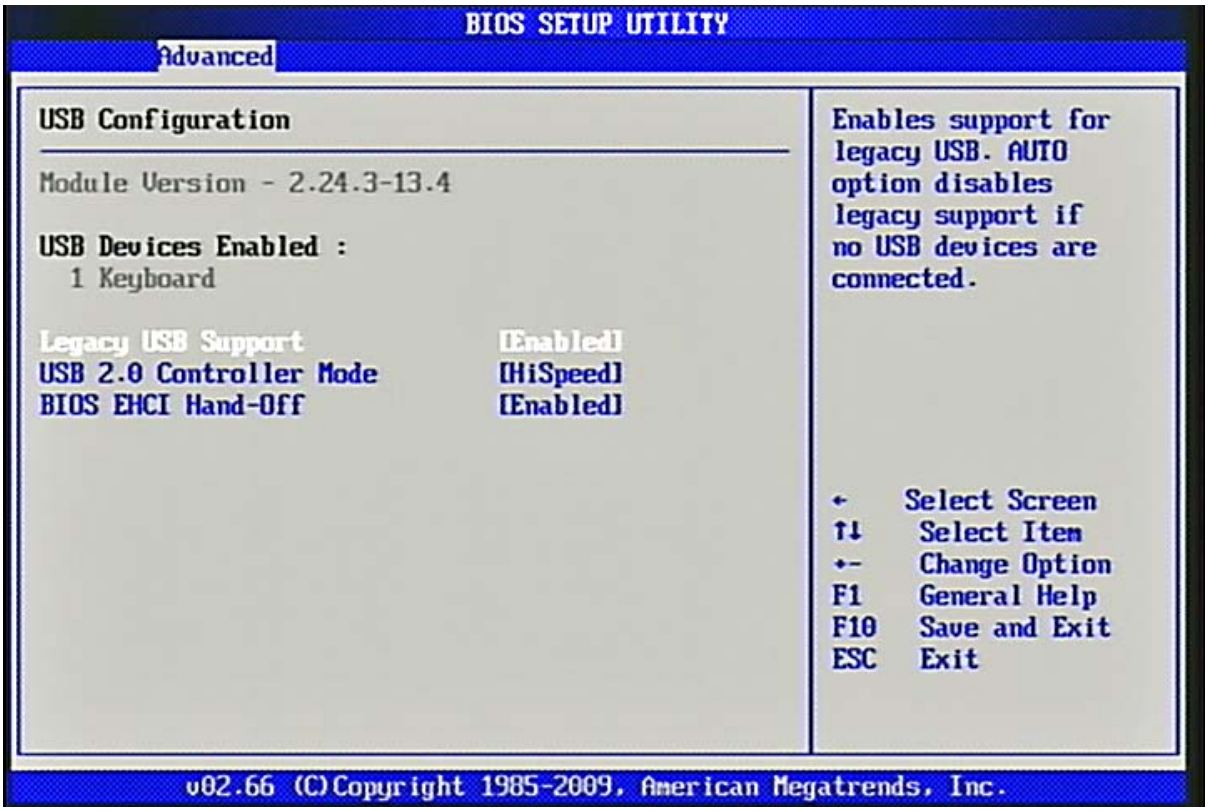


TCG/TPM SUPPORT

Enable/Disable TPM TCG (TPM 1.1/1.2) support in BIOS

The choice: No, Yes.

USB Configuration


BIOS SETUP UTILITY
Advanced
USB Configuration
Module Version - 2.24.3-13.4
USB Devices Enabled :
1 Keyboard
Legacy USB Support [Enabled]
USB 2.0 Controller Mode [HiSpeed]
BIOS EHCI Hand-Off [Enabled]
Enables support for legacy USB. AUTO option disables legacy support if no USB devices are connected.
← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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Legacy USB Support

Set to [Enabled] if you need to use any USB 1.1/2.0 device in the operating system that does not support or have any USB 1.1/2.0 driver installed, such as DOS and SCO Unix.

The choice: Disabled, Enabled, Auto.

USB 2.0 Controller Mode

This setting specifies the operation mode of the onboard USB 2.0 controller.

The choice: FullSpeed, HiSpeed.

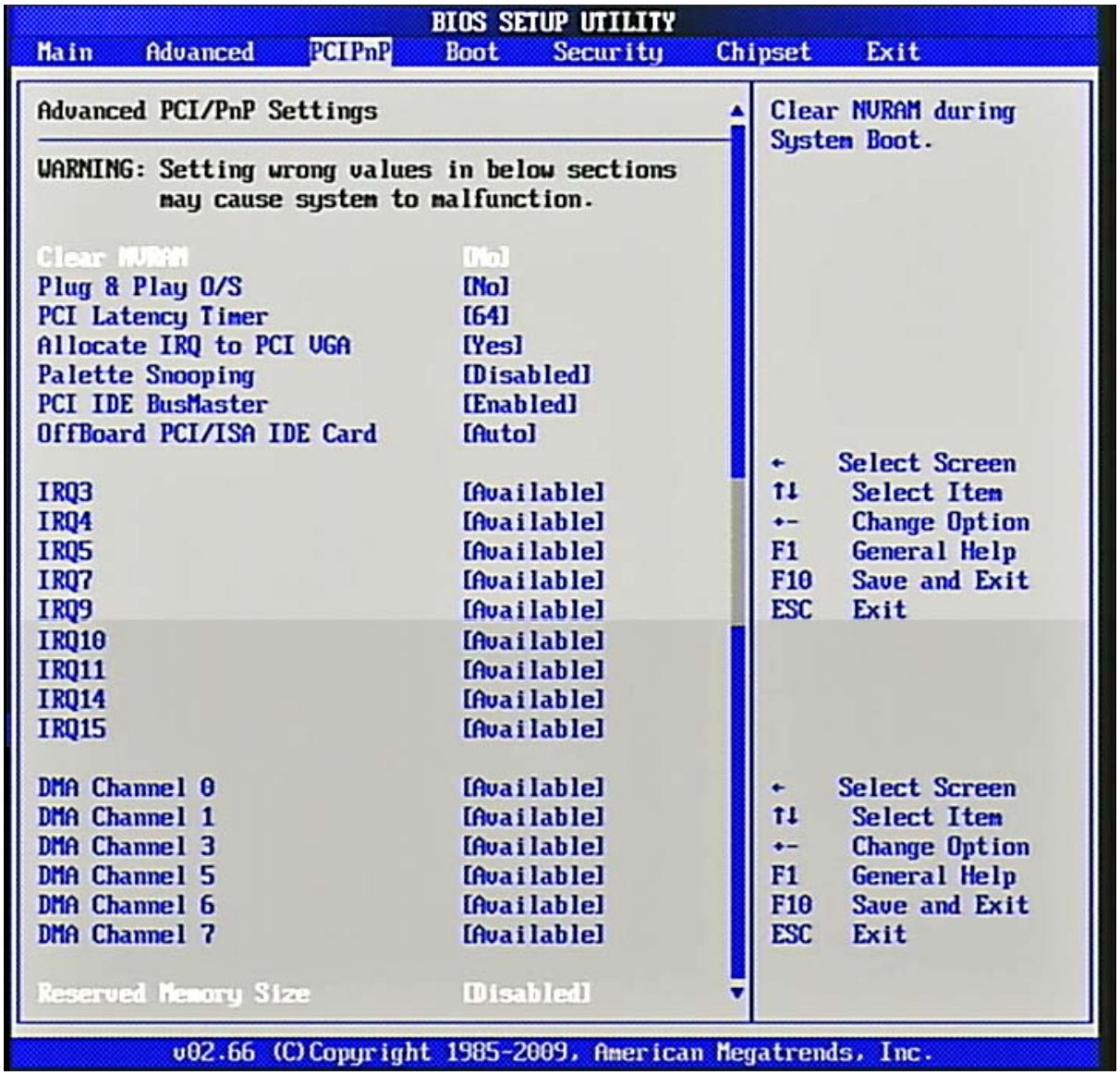
BIOS EHCI Hand-Off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.

The choice: Disabled, Enabled.

4.4 PCIPnP

Advanced PCI/PnP setting wrong values in below sections may cause system to malfunction.



Clear NVRAM

Clear NVRAM during System Boot.

The choice: No, Yes.

Plug & Play O/S

No: lets the BIOS configure all the devices in the system.
Yes: lets the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.

The choice: No, Yes.

PCI Latency Timer

Select value in units of PCI clocks for PCI device latency timer register.

The choice: 32, 64, 96, 128, 160, 192, 224, 248.

Allocate IRQ to PCI VGA

Yes: Assigns IRQ to PCI VGA card if card requests an IRQ.
No: Does not assign IRQ to PCI VGA card even if card requests an IRQ.

The choice: No, Yes.

Palette Snooping

Enabled: informs the PCI devices that an ISA graphics device is installed in the system so the card will function correctly.

The choice: Disabled, Enabled.

PCI IDE BusMaster

Enabled: Uses PCI bus mastering for reading / writing to IDE drives.

The choice: Disabled, Enabled.

OffBoard PCI/ISA IDE Card

Some PCI IDE cards may require this to be set to the PCI slot number that is holding the card. AUTO: Works for most PCI IDE cards

The choice: Auto, PCI Slot1, PCI Slot2, PCI Slot3, PCI Slot4, PCI Slot5, PCI Slot6.

IRQ 3 / IRQ 4 / IRQ5 / IRQ7 / IRQ 9 / IRQ 10 / IRQ 11 / IRQ 14 / IRQ 15

Available: Specified IRQ is available to be used by PCI/PnP devices.
Reserved: Specified IRQ is reserved for used by Legacy ISA devices.

The choice: Available, Reserved.

DMA Channel 0 / DMA Channel 1 / DMA Channel 3 / DMA Channel 5 / DMA Channel 6 / DMA Channel 7

Available: Specified DMA is available to be used by PCI/PnP devices.
Reserved: Specified DMA is reserved for use by Legacy ISA devices.

The choice: Available, Reserved.

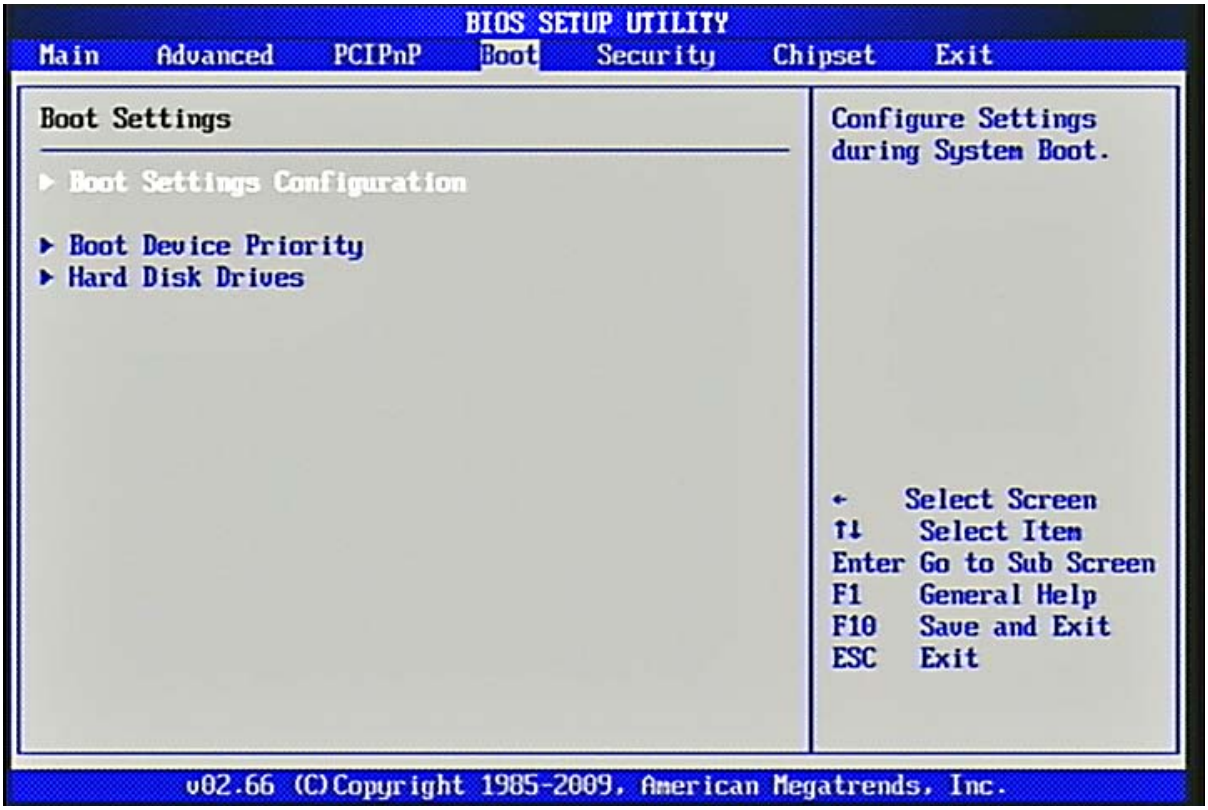
Reserved Memory Size

Select Size of memory block to reserve for legacy ISA devices.

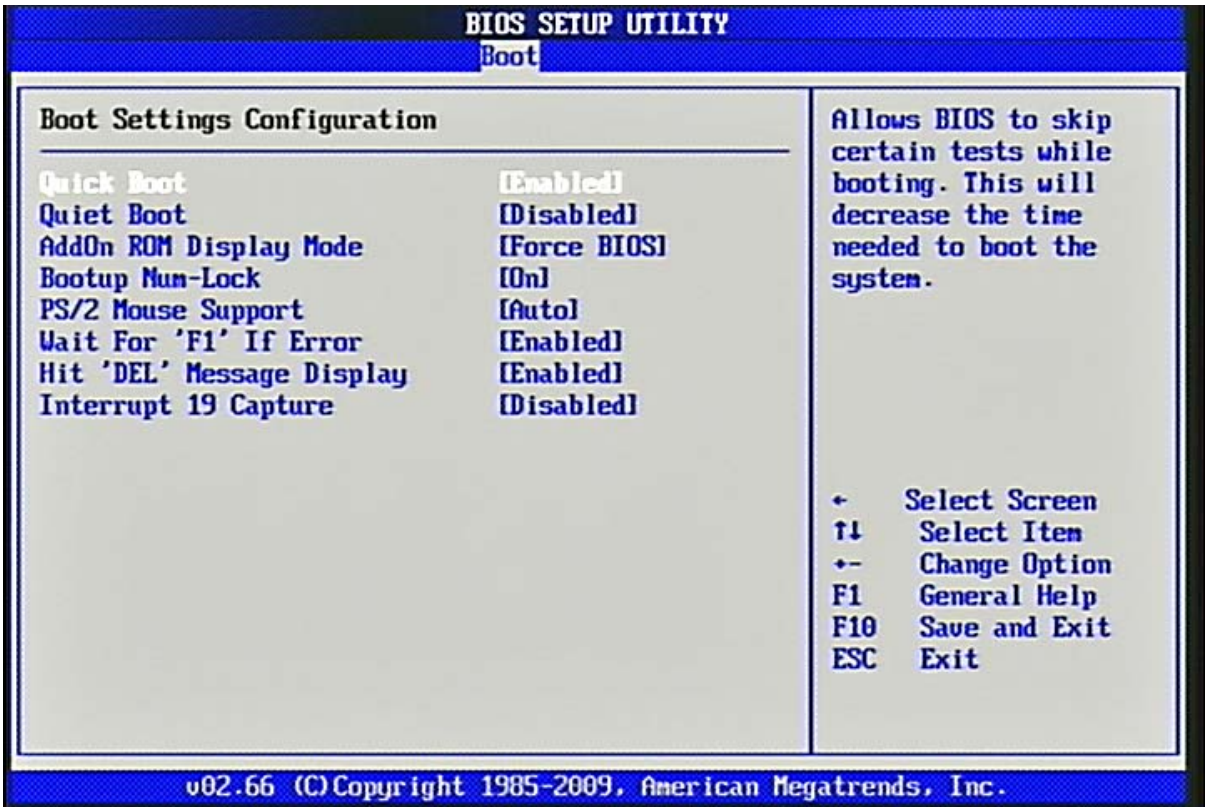
The choice: Disabled, 16K, 32K, 64K.

4.5 Boot

Use this menu to specify the priority of boot devices.



Boot Settings Configuration


BIOS SETUP UTILITY
Boot
Boot Settings Configuration
Quick Boot [Enabled]
Quiet Boot [Disabled]
AddOn ROM Display Mode [Force BIOS]
Bootup Num-Lock [On]
PS/2 Mouse Support [Auto]
Wait For 'F1' If Error [Enabled]
Hit 'DEL' Message Display [Enabled]
Interrupt 19 Capture [Disabled]
Allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system.
← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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Quick Boot

Enabling this setting will cause the BIOS power-on self test routine to skip some of its tests during boot up for faster system boot.

The choice: Disabled, Enabled.

Quiet Boot

This BIOS feature determines if the BIOS should hide the normal POST messages with the motherboard or system manufacturer's full-screen logo. When it is enabled, the BIOS will display the full-screen logo during the boot-up sequence, hiding normal POST messages.
When it is disabled, the BIOS will display the normal POST messages, instead of the full-screen logo.

Please note that enabling this BIOS feature often adds 2-3 seconds of delay to the booting sequence. This delay ensures that the logo is displayed for a sufficient amount of time. Therefore, it is recommended that you disable this BIOS feature for a faster boot-up time.

The choice: Disabled, Enabled.

AddOn ROM Display Mode

This item is used to determine the display mode when an optional ROM is initialized during POST. When set to [Force BIOS], the display mode used by AMI BIOS is used. Select [Keep Current] if you want to use the display mode of optional ROM.

The choice: Force BIOS, Keep Current.

Bootup Num-Lock

This setting is to set the Num Lock status when the system is powered on.
Setting to [On] will turn on the Num Lock key when the system is powered on.
Setting to [Off] will allow users to use the arrow keys on the numeric keypad.

The choice: Off, On.

PS/2 Mouse support

Select [Enabled] if you need to use a PS/2-interfaced mouse in the operating system.

The choice: Disabled, Enabled, Auto.

Wait For 'F1' If Error

When this setting is set to [Enabled] and the boot sequence encounters an error, it asks you to press F1. If disabled, the system continues to boot without waiting for you to press any keys.

The choice: Disabled, Enabled.

Hit 'DEL' Message Display

Set this option to [Disabled] to prevent the message as follows:

Hit Del if you want to run setup

It will prevent the message from appearing on the first BIOS screen when the computer boots. Set it to [Enabled] when you want to run the BIOS Setup Utility.

The choice: Disabled, Enabled.

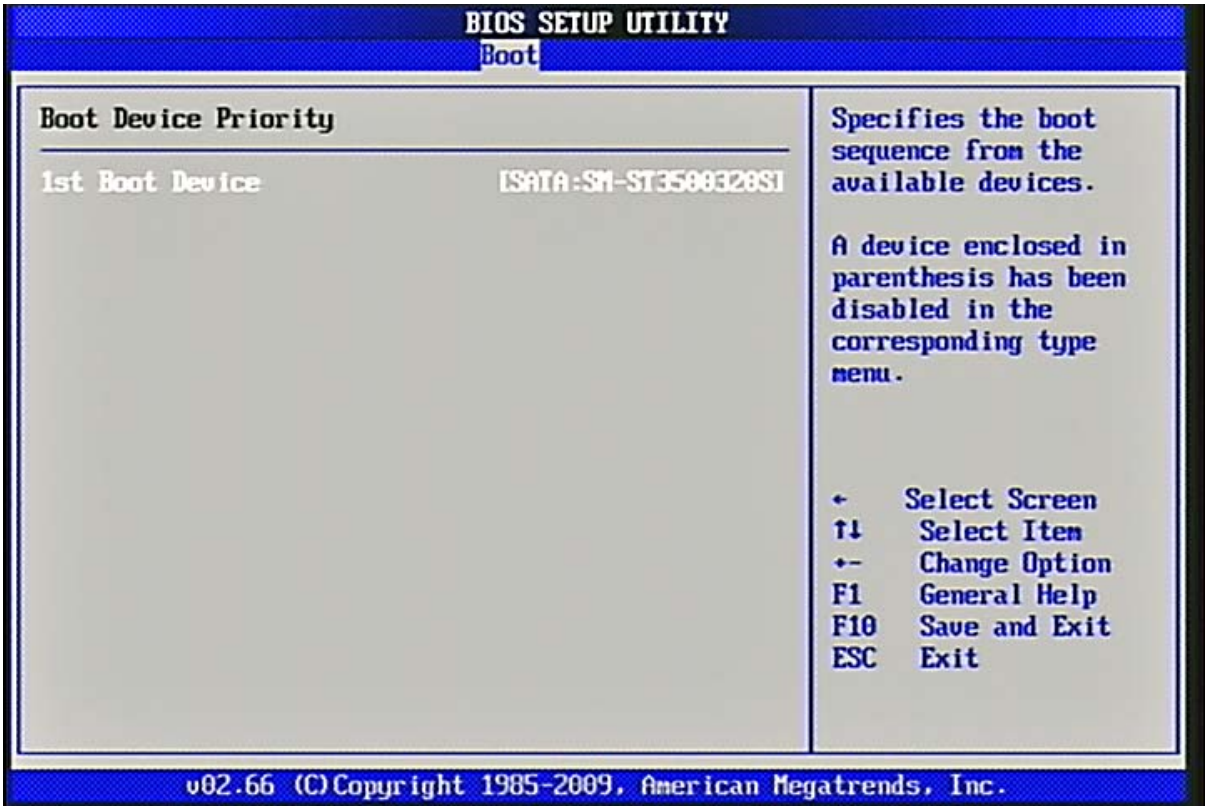
Interrupt 19 Capture

Interrupt 19 is the software interrupt that handles the boot disk function. When enabled, this BIOS feature allows the ROM BIOS of these host adaptors to "capture" Interrupt 19 during the boot process so that drives attached to these adaptors can function as bootable disks. In addition, it allows you to gain access to the host adaptor's ROM setup utility, if one is available.

When disabled, the ROM BIOS of these host adaptors will not be able to "cap ture" Interrupt 19. Therefore, you will not be able to boot operating systems from any bootable disks attached to these host adaptors. Nor will you be able to gain access to their ROM setup utilities.

The choice: Disabled, Enabled.

Boot Device Priority


BIOS SETUP UTILITY
Boot
Boot Device Priority
1st Boot Device
[SATA:SM-ST3500320S]
Specifies the boot sequence from the available devices.
A device enclosed in parenthesis has been disabled in the corresponding type menu.
← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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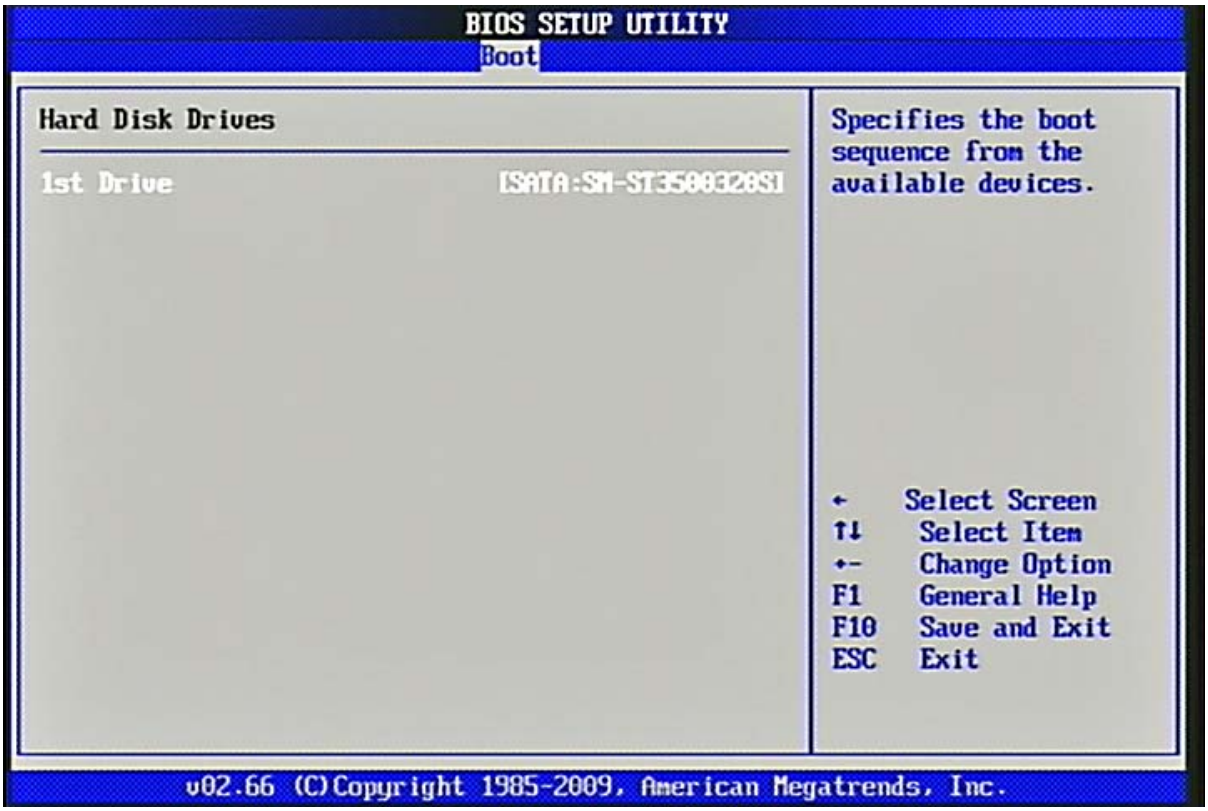
1st Boot Device

The items allow you to set the sequence of boot devices where BIOS attempts to load the disk operating system. First press <Enter> to enter the sub-menu. Then you may use the arrow keys (↑ ↓) to select the desired device, then press <+>, <—> or <PageUp>, <PageDown> key to move it up/down in the priority list.

The choice: (Network: IBA GE Slot 00C8 v1324), Disabled.

Hard Disk Drives

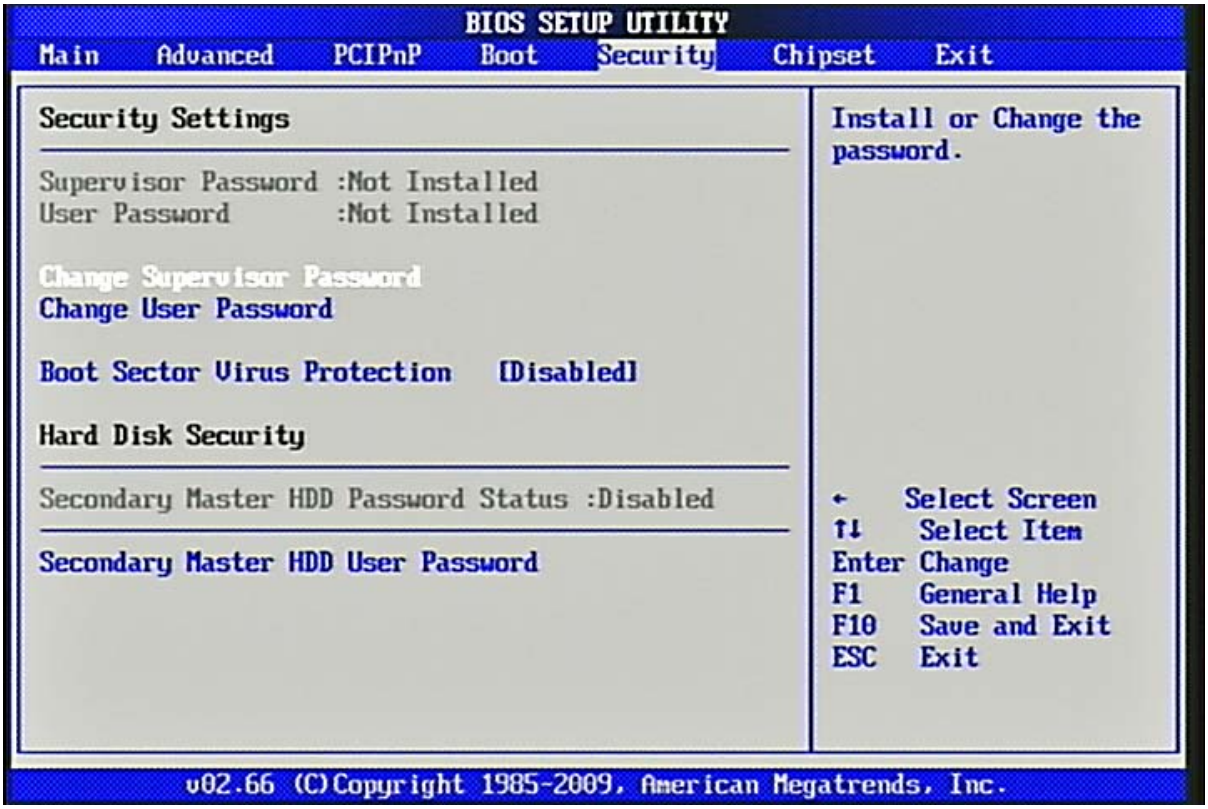


1st Drive

This setting allows users to set the priority of the removable devices. First press <Enter> to enter the sub-menu. Then you may use the arrow keys (↑ ↓) to select the desired device, then press <+>, <—> or <PageUp>, <PageDown> key to move it up/down in the priority list.

4.6 Security

Use this menu to set supervisor and user passwords.



Supervisor Password / Change Supervisor Password

Supervisor Password controls access to the BIOS Setup utility. These settings allow you to set or change the supervisor password.

User Password / Change User Password

User Password controls access to the system at boot. These settings allow you to set or change the user password.

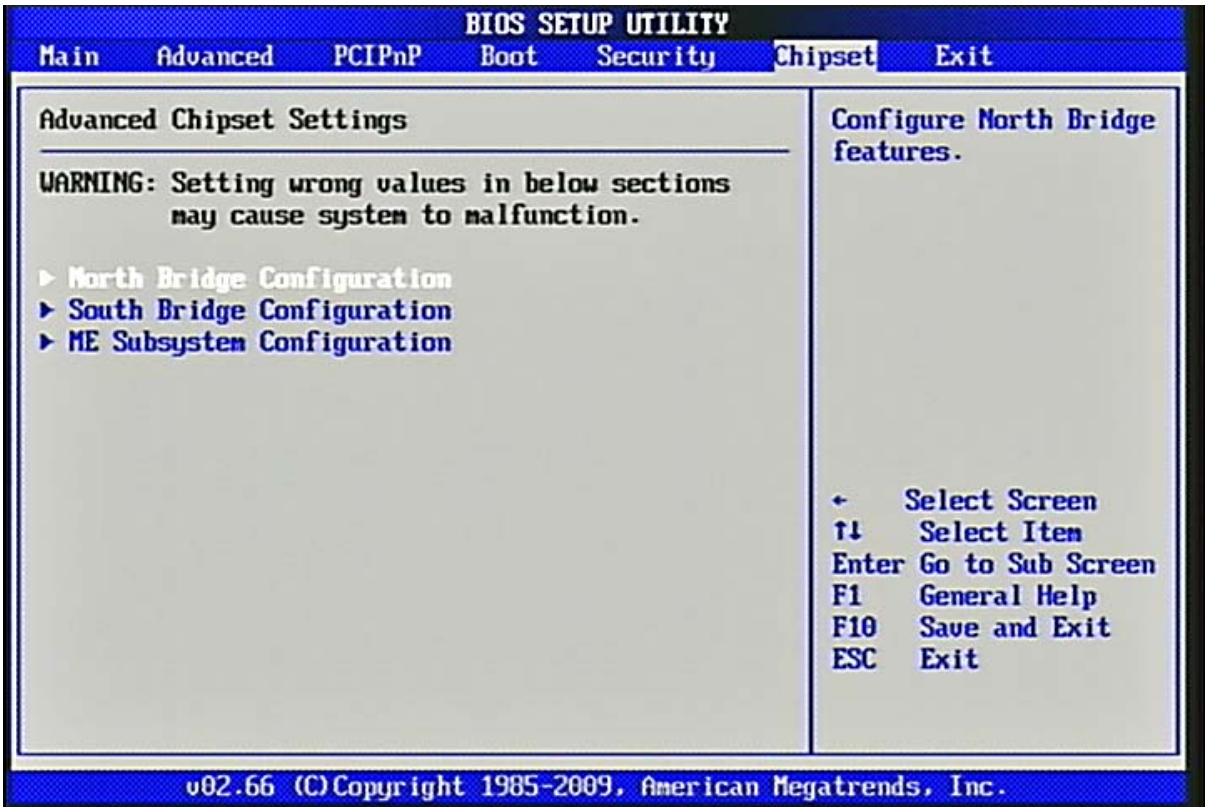
Boot Sector Virus Protection

Boot Sector Virus Protection.

The choice: Disabled, Enabled.

4.7 Chipset

This menu controls the advanced features of the onboard Northbridge and Southbridge.


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Advanced Chipset Settings
WARNING: Setting wrong values in below sections may cause system to malfunction.
North Bridge Configuration
South Bridge Configuration
ME Subsystem Configuration
Configure North Bridge features.
← Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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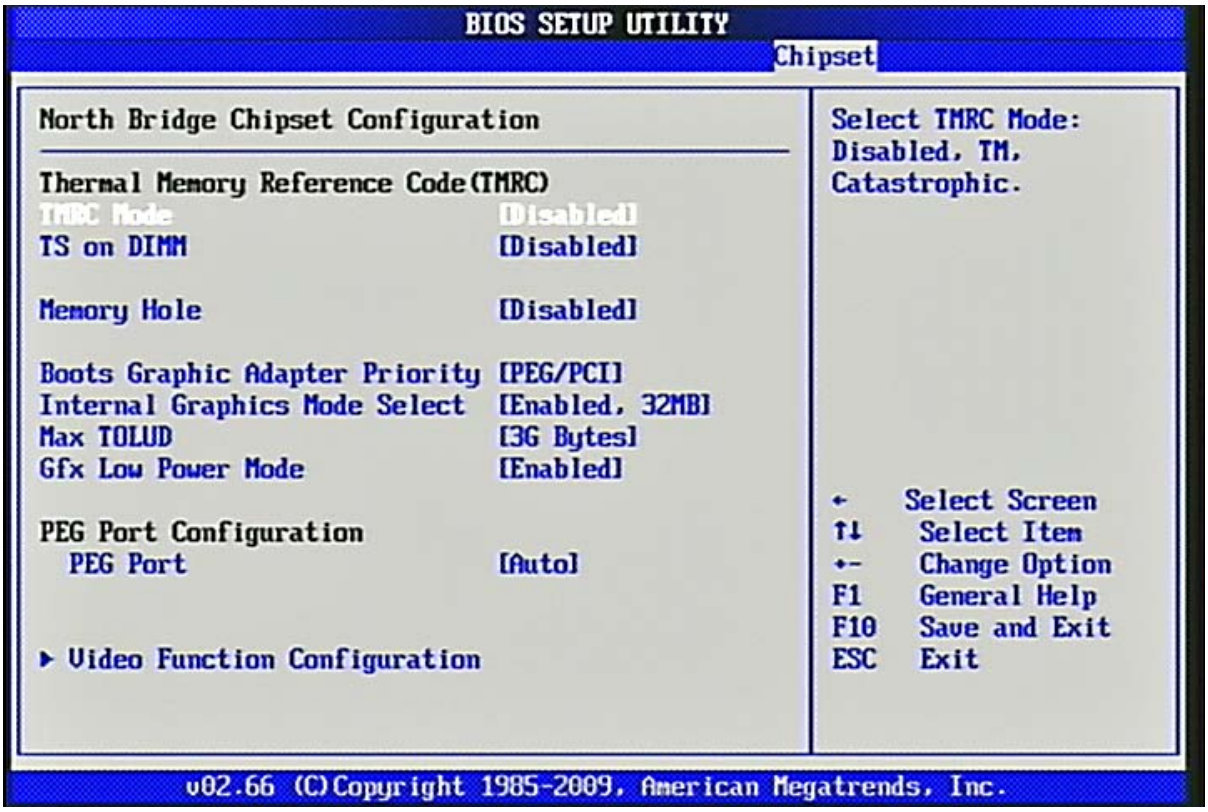
North Bridge Chipset Configuration



TMRC Mode

Select TMRC Mode

The choice: Disabled, Enabled.

TS on DIMM

Disabled/Enabled Thermal Sensor on DIMM.

The choice: Disabled, Enabled.

Memory Hole

In order to improve performance, certain space in memory is reserved for ISA cards. This memory must be mapped into the memory space below 16MB.

The choice: Disabled, 15MB-16MB.

Boots Graphic Adapter Priority

Select which graphics controller to use as the primary boot device.

The choice: IGD, PCI/IGD, PCI/PEG, PEG/IGD, PEG/PCI.

Internal Graphics Mode Select

Select the amount of system memory used by the internal graphics device.

The choice: Enabled, 32MB, Enabled, 64MB, Enabled, 128MB.

Max TOLUD

Maximum Value of TOLUD

The choice: 3G Bytes, 2.5G Bytes, 2G Bytes

GFx Low Power Mode

This option is applicable for SFF only

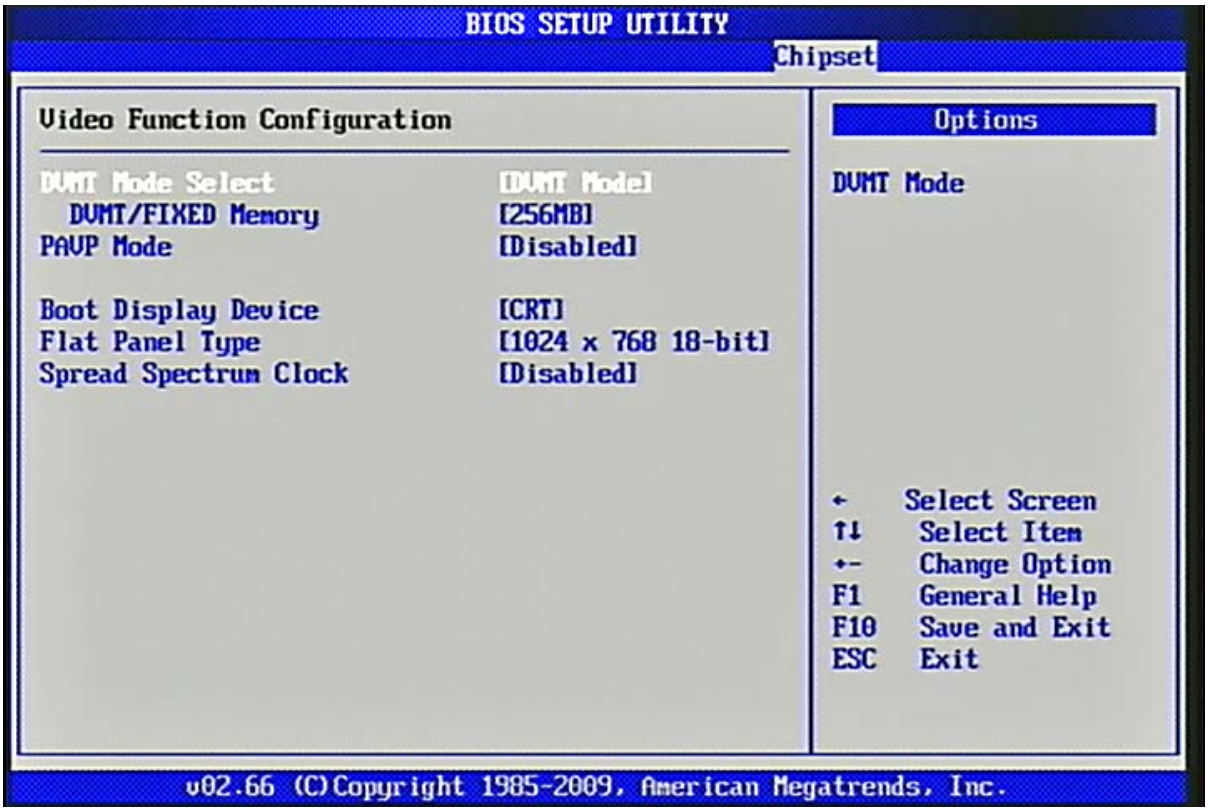
The choice: Disabled, Enabled.

PEG Port

This setting allows you to select whether to use the on-chip graphics processor or the PCI Express card. When set to [Auto], the BIOS checks to see if a PCI Express graphics card is installed. If it detects that a PCI Express graphics card is present, the motherboard boots up using that card. Otherwise, it defaults to the onboard graphics processor.

The choice: Auto, Disabled.

Video Function Configuration



DVMT Mode Select

Intel's Dynamic Video Memory Technology (DVMT) allows the system to dynamically allocate memory resources according to the demands of the system at any point in time. The key idea in DVMT is to improve the efficiency of the memory allocated to either system or graphics processor.

It is recommended that you set this BIOS feature to DVMT Mode for maximum performance. Setting it to DVMT Mode ensures that system memory is dynamically allocated for optimal balance between graphics and system performance.

The choice: Fixed Mode, DVMT Mode.

DVMT/FIXED Memory

When set to DVMT/FIXED Mode, the graphics driver will allocate a fixed amount of memory as dedicated graphics memory, as well as allow more system memory to be dynamically allocated between the graphics processor and the operating system.

The choice: 128MB, 256MB.

PAVP Mode

GMCH Protected Audio Video Path (PAVP) BIOS Support.

The choice: Disabled, Lite, High.

Boot Display Device

The choice: CRT, LVDS, CRT+LVDS.

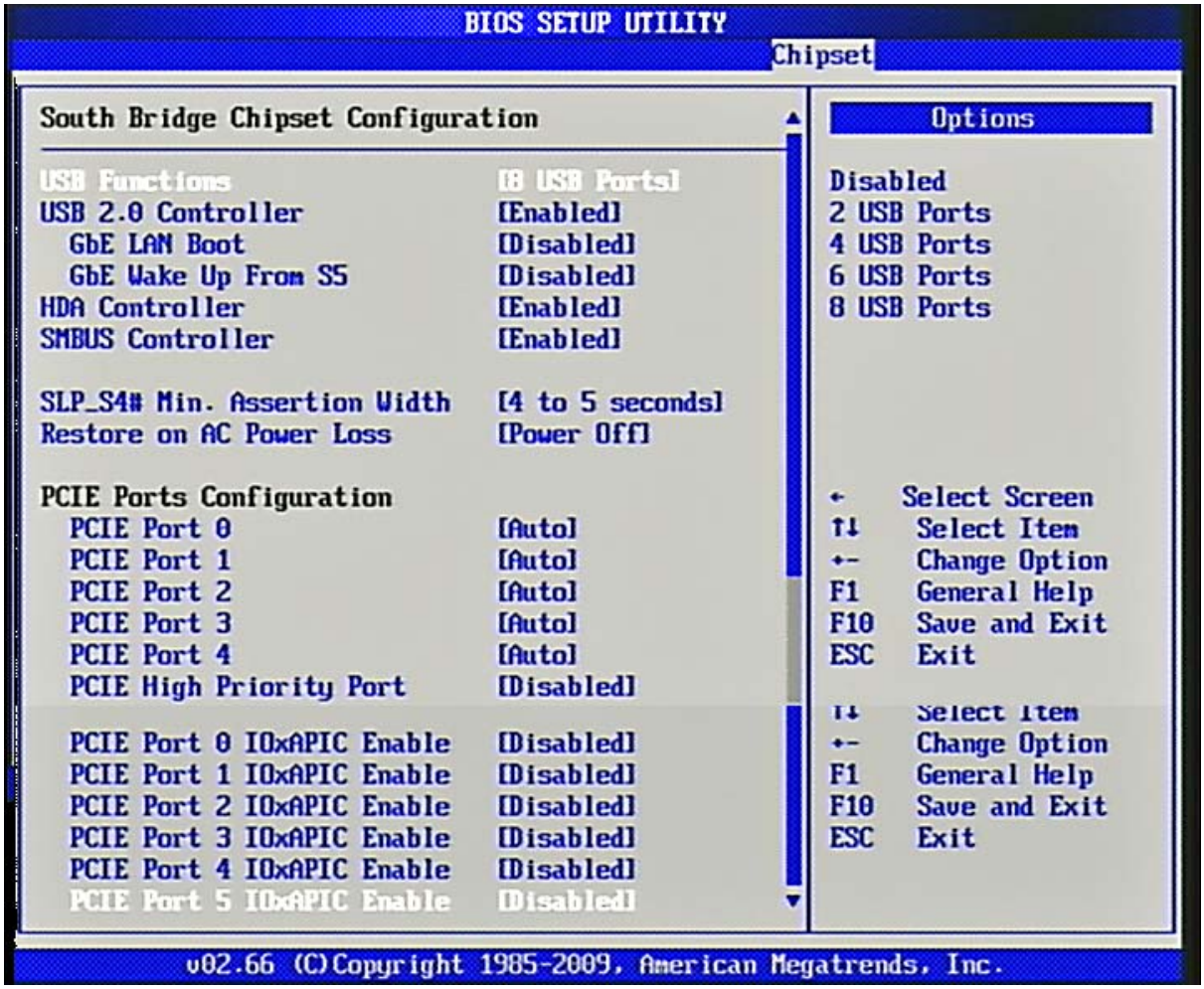
Flat Panel Type

The choice: 640x480 18 bit, 800x600 18 bit, 1024x768 18 bit, 1280x1024 18bit, 1400x1050 18 bit, 1600x1200 18bit, 800x600 24 bit, 1024x768 24 bit, 1280x1024 24 bit.

Spread Spectrum Clock

The choice: Disabled, Enabled.

South Bridge Configuration



USB Functions

This setting specifies the function of the onboard USB controller.

The choice: Disabled, 2 USB Ports, 4 USB Ports, 6 USB Ports.

USB 2.0 Controller

Set to [Enabled] if you need to use any USB 2.0 device in the operating system that does not support or have any USB 2.0 driver installed, such as DOS and SCO Unix.

GbE LAN Boot

When [Enabled], the BIOS attempts to boot from a LAN boot image before it attempts to boot from a local storage device.

The choice: Enabled, Disabled.

GbE Wake Up From S5

This field specifies whether the system will be awakened from the S5 power saving mode when activity or input signal of onboard LAN is detected.

The choice: Enabled, Disabled.

HDA Controller

This setting controls the High Definition Audio interface integrated in the Southbridge.

The choice: Enabled, Disabled.

SMBUS Controller

The choice: Enabled, Disabled.

SLP_S4# Min. Assertion Width

The choice: 4 to 5 seconds, 3 to 4 seconds, 2 to 3 seconds, 1 to 2 seconds.

Restore on AC Power Loss

This item allows user to configure the power status of using ATX power supply after a serious power loss occurs.

The choice: Power Off, Power On, Last State.

PCIE Port 0/ Port 1/ Port 2/ Port 3/ Port 4

The choice: Auto, Enabled, Disabled.

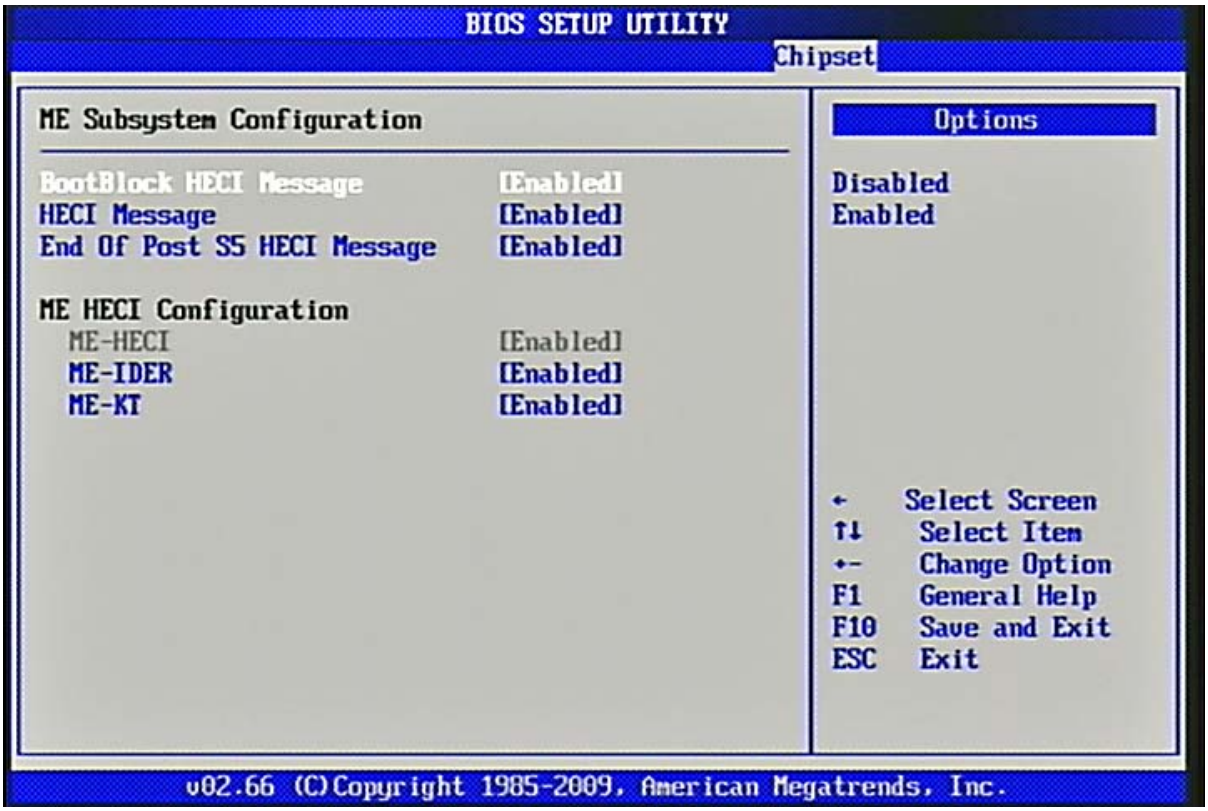
PICE High Priority Port

The choice: Disable, Port 0, Port 1, Port 2, Port 3, Port 4, Port 5.

PICE Port 0/1/2/3/4/5 IOxAPIC Enable

The choice: Enabled, Disabled.

ME Subsystem Configuration



BootBlock HECI Message

The choice: Disabled, Enabled.

HECI Message

The choice: Disabled, Enabled.

End Of Post S5 HECI Message

The choice: Disabled, Enabled.

ME-IDER

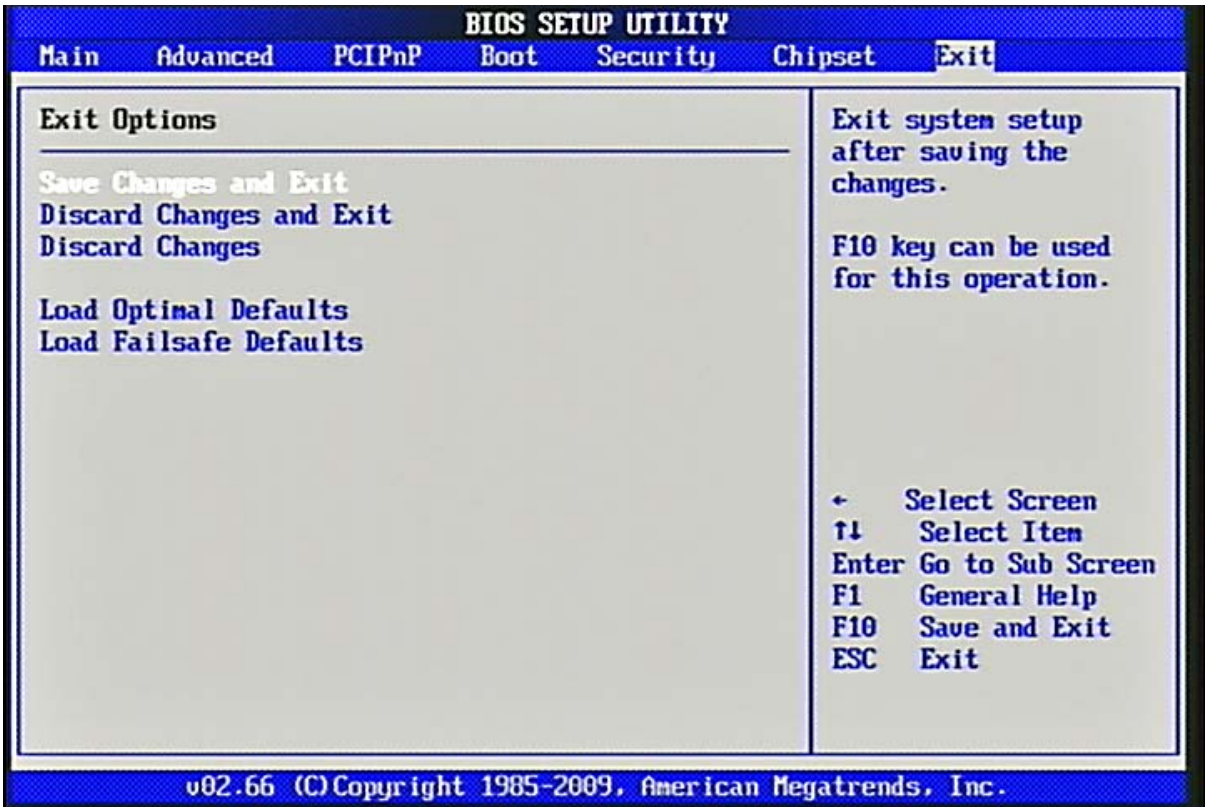
The choice: Disabled, Enabled.

ME-KT

The choice: Disabled, Enabled.

4.8 Exit

This menu allows you to load the BIOS default values or factory default settings into the BIOS and exit the BIOS setup utility with or without changes.


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Exit Options
Save Changes and Exit
Discard Changes and Exit
Discard Changes
Load Optimal Defaults
Load Failsafe Defaults
Exit system setup after saving the changes.
F10 key can be used for this operation.
← Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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Exit Saving Changes

Exit System Setup and save your changes to CMOS. Pressing <Enter> on this item asks for confirmation: Save changes to CMOS and exit the Setup Utility.

Discard Changes and Exit

Abandon all changes and exit the Setup Utility.

Discard Changes

Abandon all changes and continue with the Setup Utility.

Load Optimal Defaults

Use this menu to load the default values set by the SBC manufacturer specifically for optimal performance of the SBC.

Load Failsafe Defaults

Use this menu to load the default values set by the BIOS vendor for stable system performance.

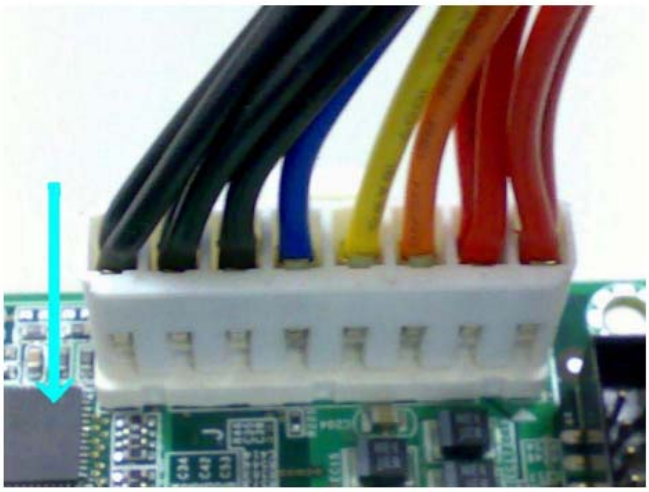
Chapter 5
Troubleshooting

This chapter provides a few useful tips to quickly get NANO-8050 running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will primarily focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

5.1 Hardware Quick Installation

ATX Power Setting

Unlike other Single board computer, NANO-8050 supports ATX only. Therefore, there is no other setting that really needs to be set up. However, there are only two connectors that must be connected—J9 (8 pins Power Connector) Figure.



5.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the device cables required before turning on ATX power. 200-pin DDR2 SO-DIMM, keyboard, mouse, PATA hard disk, VGA connector, device power cables, ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with NANO-8050, it is recommended, when going with the boot-up sequence, to hit "DEL" key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to "**Load Optimal Defaults**", press "Enter" and "Y" to load in default optimal BIOS setup. This will force your BIOS setting back to the initial factory configuration. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting any time when system appears to be unstable in boot up sequence.

Auto Detect Hard Disks

In the BIOS => Standard CMOS setup menu, pick up any one from Primary/Secondary Master/Slave IDE ports, and press "Enter". Setup the selected IDE port and its access mode to "Auto". This will force system to automatically pick up the IDE devices that are being connected each time system boots up.

Improper disable operation

There are too many occasions where users disable a certain device/feature in one application through BIOS setting. These variables may not be set back to the original values when needed. These devices/features will certainly fail to be detected. It is also very common that users would like to disable a certain device/port to release IRQ resource. A few good examples are

A quick review of the basic IRQ mapping is given below for your reference.

IRQ#	Description
IRQ #0	System Timer
IRQ #1	Keyboard Event
IRQ #2	Usable IRQ
IRQ #3	Usable IRQ
IRQ #4	COM1
IRQ #5	Usable IRQ
IRQ #6	Diskette Event
IRQ #7	Usable IRQ
IRQ #8	Real-Time Clock
IRQ #9	Usable IRQ
IRQ #10	Usable IRQ
IRQ #11	Usable IRQ
IRQ #12	IBM Mouse Event
IRQ #13	Coprocessor Error
IRQ #14	Hard Disk Event
IRQ #15	Usable IRQ

It is then very easy to find out which IRQ resource is ready for additional peripherals. If IRQ resource is not enough, please disable some devices listed above to release further IRQ numbers.

5.3 FAQ

Symptom: SBC keeps beeping, and no screen has shown.

Solution: In fact, each beep sound represents different definition of error message. Please refer to table as following:

Beep sounds	Meaning	Action
One long beep with one short beeps	DRAM error	Change DRAM or reinstall it
One long beep constantly	DRAM error	Change DRAM or reinstall it
One long beep with two short beeps	Monitor or Display Card error	Please check Monitor connector whether it inserts properly
Beep rapidly	Power error warning	Please check Power mode setting

Information & Support

Question:I forget my password of system BIOS, what am I supposed to do?

Answer: You can simply short 2-3 pins on JP5 to clean your password.

Note:
Please visit our technical web site at
http://www.portwell.com.tw
For additional technical information, which is not covered in this manual, you can mail to tsd@mail.portwell.com.tw or you can also send mail to our sales, they wull be very delighted to forward them to us.

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used for your reference.

Memory Area	Size	Device Description
0000 – 0XXX	XXK	XXX
0000-003F	1K	Interrupt Area
0040-004F	0.3K	BIOS Data Area
0050-006F	0.5K	System Data
0070-0E2E	54K	DOS
0E2F-0F6B	5K	Program Area
0F6C-9DBF	563K	[Available]
First Meg	-- Conventional memory end at 631K --	
A000-AXXX	XX K	XXX
9DC0-9DFF	1K	Extended BIOS Area
9E00-9FFF	8K	Unused
A000-AFFF	64K	VGA Graphics
B000-B7FF	32K	Unused
B800-BFFF	32K	VGA Text
C000-CAFF	63K	Video ROM
CFE0-EFFF	128K	Unused
F000-FFFF	64K	System ROM

Interrupt Request Lines (IRQ)

Peripheral devices can use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

IRQ#	Current Use	Default Use
IRQ 0	System ROM	System Timer
IRQ 1	System ROM	Keyboard Event
IRQ 2	[Unassigned]	Usable IRQ
IRQ 3	[Unassigned]	Usable IRQ
IRQ 4	System ROM	COM1
IRQ 5	[Unassigned]	Usable IRQ
IRQ 6	System ROM	Diskette Event
IRQ 7	Unesed	Usable IRQ
IRQ 8	System ROM	Real-Time Clock
IRQ 9	[Unassigned]	Usable IRQ
IRQ 10	[Unassigned]	Usable IRQ
IRQ 11	[Unassigned]	Usable IRQ
IRQ 12	System ROM	IBM Mouse Event
IRQ 13	System ROM	Coprocessor Error
IRQ 14	System ROM	Hard Disk Event
IRQ 15	[Unassigned]	Usable IRQ